HIGH QUALITY SUB-MICRON Nb TRILAYER TUNNEL JUNCTIONS FOR A 100 GHz SIS RECEIVER

A.H. Worsham and D.E. Prober
Dept. of Applied Physics, Yale University
P.O. Box 2157 Yale Station
New Haven, CT 06520

J.H. Kang and J.X. Przybysz
Westinghouse Science and Technology Center
Pittsburgh, PA 15235

M.J. Rooks
National Nanofabrication Facility
Knight Lab, Cornell University
Ithaca, NY 14853

Abstract

A modified SNIP process was used to fabricate high quality 0.5, 2, and 4 $(\mu m)^2$ small area $Nb/AlO_x/Nb$ trilayer tunnel junctions with current densities as large as 5000 A/cm^2. The *average* junction quality factors for the junctions at 4.4K were $V_m(2mV)=39$ mV for $J_c=3000$ A/cm^2 and $V_m(2mV)=27$ mV for $J_c=5000A/cm^2$. The best values of V_m obtained were 50 mV for $J_c=3000$ A/cm^2 and 41 mV for $J_c=5000$ A/cm^2. These devices were designed and fabricated for use in a W band mixer receiver. The substrate was 50μm thick fused or crystal quartz. Special methods were developed for handling such thin insulating substrates and patterning films. The fabrication process was self-aligned and used SiO_2 instead of anodized Nb as the thick insulator. SiO_2 isolated the junction area and defined the opening for contact to the Nb wiring layer. We have fabricated series arrays of up to 12 junctions, with individual junction areas of 0.5 $(\mu m)^2$. The array I-V quality was not degraded compared to that of an individual junction.

Introduction

SIS (superconductor-insulator-superconductor) tunnel junctions are important heterodyne (mixing) elements at high frequencies.[1,2] In order to operate in the low noise quantum regime, the device I-V characteristic needs to be "sharp" on the scale of the photon energy; the non-linearity at the sum gap must be smaller than the width of the photon induced step on the I-V curve, $\Delta V = \hbar\omega/e \approx 400$ μV at 100 GHz. In addition to this I-V requirement, the sub-gap leakage current should be small in order to limit shot noise contributions to the overall receiver noise. A useful SIS mixer device should also have other features including ruggedness, lack of aging, low specific capacitance, and operation at 4.2K. The device should also thermally cycle. $Nb/AlO_x/Nb$ trilayer tunnel junctions possess these qualities. Since the introduction of $Nb/AlO_x/Nb$ trilayers[3] in 1983, they have been shown to be capable of near-ideal current voltage characteristics[4] and to be compatible with small area fabrication technology.[5] In particular, small, (1.5 μm x 1.5 μm) Nb trilayer tunnel junctions are currently used as mixer receiver detection elements.[6] Nb trilayers have shown no aging affects in ambient temperature storage.[7]

For use as 100 GHz SIS mixer junctions, the Nb trilayer device fabrication must achieve reproducible, small area ($<2\mu m^2$) tunnel junctions with low overlap capacitance between the Nb wiring layer and trilayer. Since low overlap capacitance was desired, technologies using Nb_2O_5 produced by anodization[3,5,8,9] were undesirable. We chose instead to use a modified selective niobium insulation process (SNIP),[10,11] which used SiO_2 ($\varepsilon=3.8$) to isolate the junction areas. This process was general and would be useful whenever small, high quality tunnel junctions are necessary.

Processing

The general layout of the devices was as follows. The substrate was 25.4 mm x 25.4 mm x 50 μm fused or crystal quartz.[12] This thickness was chosen based on scale modelling of the mixer microstripline circuitry. The scale modelling showed that substrates thicker than 50 μm gave radiative losses. This could be due to higher modes in the substrate. Each substrate contained 102 chips of size 1mm x 4 mm. Each individual chip had 1 to 12 junctions in series, *dc*/*if* feedlines, and *rf* coupling structures. Some chips had a 2 μm wide microstripline inductor in *rf* parallel with the mixer junctions (the equivalent circuits are discussed in reference 18). Due to the size of the devices and layout of the receiver, the *dc* characteristics were measured in the receiver using a two probe electrical configuration. The series resistance due to the contacts was less than a few ohms and was easily discernable; this contact resistance gave a finite slope to the "zero voltage" Josephson current. Since the contact resistance was a very small fraction of the device R_n, we do not expect it to have a large effect on the high frequency results.

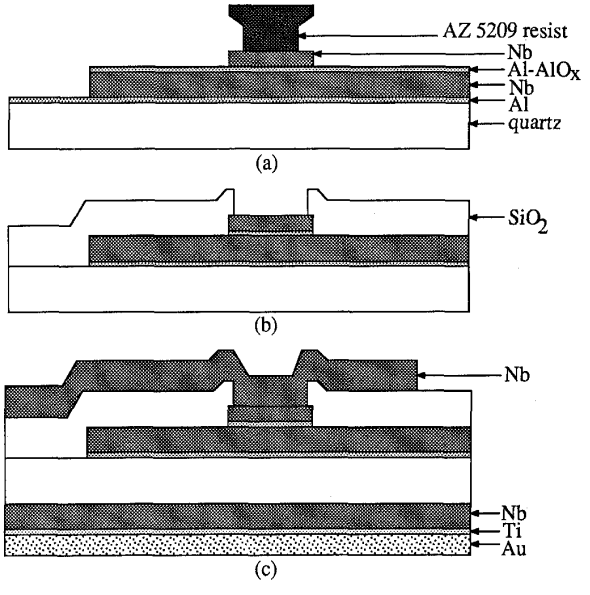

Fig. 1. Schematic diagram of the device fabrication.

The substrates employed were fragile. Usual methods of substrate handling thus proved difficult. In order to decrease breakage losses, the quartz substrate was mounted on a 0.56 mm thick silicon wafer with silicone based high vacuum grease.[13] Vacuum grease was chosen as the adhesive material since it contains no solvents which can escape and crack the substrate during photoresist baking, it provides a reasonable heat sink during sputtering, it is removable with the widely used solvent trichloroethane, and it can be made uniformly thin. Before being mounted together, the quartz and silicon wafers were solvent cleaned. Vacuum grease was then spread in the center 25.4 mm x 25.4 mm section of the silicon wafer. The cleaned quartz substrate was placed on the vacuum grease. After baking the wafers 5 minutes at 110°C, a contact mask aligner was used to press the two

Manuscript received September 24, 1990.

wafers together by slowing bringing them into contact with a mask. In this way, the grease spread uniformly underneath the quartz substrate and trapped air escaped. After this mounting procedure, the wafer composite cooled and the top surface of the quartz substrate was cleaned by spinning the composite quartz/silicon wafer on a spinner and spray solvent cleaning. All wafer cleaning during subsequent processing was done by spray solvent cleaning on a spinner in order to minimize the exposure of the vacuum grease to solvents. Normally, the quartz wafer, held down by vacuum grease, was not removed during the entire process, allowing the composite quartz/silicon wafer to be handled with standard procedures. This mounting method kept the quartz flat enough to contact print 0.7 μm linewidths without breaking the substrate during contact printing.

After mounting the quartz substrate onto the silicon carrier, 10 nm of Al was sputter deposited. This Al acted as an etch stop in future processing as shown in Fig. 1a. AZ 5218 image reversal photoresist[14] was used to define the trilayer deposition by liftoff. This eliminated the need for reactive ion etching to pattern the trilayer which can cause polymer formation.[15] The trilayer mask level contained 2 μm features. Without the thin Al layer, this 2 μm resolution was not attainable on a transparent substrate in image reversal resist. (Without the thin Al underlayer, reflections from the back side of the substrate smeared the exposure profile.) The Al is not transparent at the exposure wavelength, 365 nm, and was directly under the AZ 5218 resist. This Al layer therefore allowed us to print this mask level with 2 μm linewidths. The $Nb/AlO_x/Nb$ trilayer was deposited and oxidized in-situ. Details of the trilayer deposition are presented elsewhere.[16] The Nb layer thicknesses used were approximately 250 nm base electrode and 80 nm counter electrode. The Al layer thickness was 10 nm.

The junction area was defined using AZ 5209 (nominally 900 nm thick) as a positive photoresist; an undercut resist edge profile was obtained with a chlorobenzene soak prior to resist development.[17] The Nb counter electrode was then reactive ion etched using CCl_2F_2, with 8% Ar and 8% O_2 (see Fig. 1a). The Ar and O_2 helped to prevent the formation of polymers. The photoresist "dot" was then uniformly shrunk in an O_2 plasma. The plasma parameters were 300 mTorr of O_2 and 50 Watts power. Although this O_2 shrink process did not change the size of the photoresist "dot" dramatically, it proved necessary in order to achieve good device quality. The oxygen plasma may passivate the exposed edges of the counter electrode, thus eliminating conduction paths which would have been available should the edges of the counter-electrode not have been covered during the subsequent SiO_2 sputter deposition. The relatively high pressure of the plasma, 300 mTorr, also proved necessary for retaining the integrity of the photoresist undercut profile. Lower pressure plasmas attacked the top of the photoresist preferentially, while the 300 mTorr plasma shrank the "dot" more isotropically, as expected. After the photoresist "dot" shrinkage, the thin Al underlayer was wet etched to eliminate conduction paths which shunted the tunnel junction to other circuit elements. (The thin Al layer remained only under the remaining Nb trilayer; it was thus always electrically shunted by the trilayer.) 150 nm of SiO_2 was sputter deposited to isolate the junction (see Fig. 1b). Liftoff of the photoresist "dot" defined the contact window. During the SiO_2 sputtering, good heat sinking of the quartz/silicon wafer composite to the sputter chamber base plate with vacuum grease proved important in order to achieve liftoff of the photoresist "dot". The counter electrode was then ion beam cleaned, and a 200 nm thick Nb wiring layer, patterned by liftoff, was deposited (see Fig. 1c). After the patterning and deposition of Ti (for Au adhesion) and Au contact pads, (not shown in Fig. 1), the quartz substrate was removed from the Si host wafer by soaking in trichloroethane. The quartz wafer was then flipped over and remounted to the Si host wafer using vacuum grease as before. A 300 nm Nb ground plane and Ti/Au contact layer were sputtered onto the wafer, completing the devices (see Fig. 1c).

The quartz wafer was diced and individual device resistances were measured at room temperature. The room temperature measurement screened the chips for device flaws. The most common device flaw was inadequate "dot" liftoff, which caused the device to be an open circuit. Cold measurements of the chips were made in the mixer block. Since the block was thermally anchored to the helium bath but was in vacuum, most measurements were at 4.4 K.

Results

The devices were used as mixer receiver elements in the W band. Junctions of nominal areas 0.5, 2, and 4 $(\mu m)^2$ were fabricated. Shown in Fig. 2 is the I-V trace of a single 0.5 $(\mu m)^2$ junction. ΔV, the width of the voltage rise at the sum gap, is less than 100 μV, which is less than $\hbar\omega/e = 414$ μV, the photon voltage width at 100 GHz. All single junctions and arrays measured showed $\Delta V < 200$ μV/junction. The device with the I-V shown in Fig. 2 showed the best heterodyne results of the devices tabulated in Tab. 1.[18] To relate the device quality to those obtained by other groups, we measured the quality factor V_m defined as $V_m = I_c R_{sg}$, where I_c is the critical current of the array, and R_{sg} is the subgap resistance of the array at V= 2n mV where n is the number of junctions in the array. In devices with depressed critical currents (due to trapped flux, for example), we assumed that $I_c = 0.7\ I_g$, where I_g is the current rise at the sum gap. In order to fairly compare arrays to single junctions, V_m for the array was divided by

Table 1. Parameters of several devices. The oxidation conditions to give the quoted J_c were determined from measurements of large area devices on Si substrates. The expected R_n was calculated from the tabulated J_c and expected device area.

Device	Wafer and Chip Designation	Nominal Area of Individual Junction $(\mu m)^2$	Number of Junctions	Expected J_c (A/cm^2)	R_n (Ω)	Expected R_n From Mask Area (Ω)	V_m/junction (mV)
A	3-C2	0.5	1	5000	71	80	22
B	4-E15	0.5	2	3000	431	260	48
C	4-B13	0.5	2	3000	125	260	22
D	1-A4	0.5	3	3000	448	390	29
E	1-B5	0.5	4	3000	619	520	50
F	3-A9	2	2	5000	61	40	28
G	3-A10	2	2	5000	71	40	41
H	3-A6	4	3	5000	30	30	28
I	1-A11	4	4	3000	124	65	18

the number of junctions in the array to give V_m/junction. Tab. 1 summarizes some of our results. Measurements of large area junctions on Si substrates were used to determine the oxidation conditions to produce the current densities given in Tab. 1. These same oxidation conditions were used for processing the trilayers on quartz substrates. All substrates were processed individually at the Westinghouse Science and Technology Center. Unfortunately, we were not able to independently measure J_c of the junctions on the quartz substrates by measuring large area junctions. Included in Tab. 1 are device resistances which were expected based on the contact mask areas and oxidation conditions, as described above. Discrepancies between the designed and measured resistances indicate that the average J_c of the junctions fabricated on the quartz substrates does vary from wafer to wafer, and/or that the lithography is somewhat limited in reproducibility across the wafer; the linear dimensions vary by about ±0.2 μm. The lithography limitation can be partially overcome by further optimizing resist exposure and chlorobenzene soak parameters. Such limitations on reproducibility were expected, since "window" geometry devices of sub-micron sizes are difficult to fabricate with optical lithography.

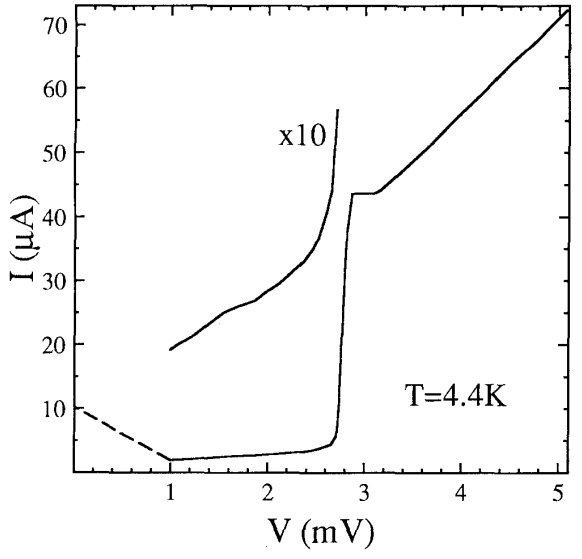

Fig. 2. I-V characteristic of device A from Tab. 1. This device showed the best hererodyne results of those measured. The dashed line indicates switching along the load line. V_m=22 mV and ΔV≈100 μV for this device.

Conclusions

Nb/AlO$_x$/Nb trilayer tunnel junctions are nearly ideal as mixer receiver elements. The high frequency mixing results, presented elsewhere[18] have shown that the device and receiver design are outstanding for microwave detection from 80-110 GHz. The fabrication process developed to produce these devices could be used whenever small, high quality, all refractory tunnel junctions are needed. The process allowed for fabrication of trilayers on thin (50μm) quartz substrates. Also important was the patterning of the trilayer by liftoff rather than reactive ion etching. In addition, the use of SiO_2, instead of the more common Nb_2O_5, is preferable when overlap capacitance is undesirable. This process should be suitable for higher frequency mixing applications where device dimensions and fabrication become more demanding. With proper design of the *rf* coupling structures, the smallest devices described here, 0.5 $(\mu m)^2$, should show quantum mixing effects at frequencies up to 600 GHz, where $\omega R_n C \approx 7$.[1] Finally, the fabrication process used only standard photolithography.

The authors would like to thank D. Winkler, N.G. Ugras, N.R. Erickson, and P.F. Goldsmith for design help and useful discussions. We also wish to thank Thermocarbon Inc., Casselberry, FL and H. Dang for the wafer dicing. This work was supported by NSF ECS-8604350 and AFOSR-88-0270. A.H. Worsham was supported in part by an IBM fellowship.

References

1. J.R. Tucker and M.J. Feldman, "Quantum detection at millimeter wavelengths," *Rev. Mod. Phys.*, 57, 1055-1113, 1985.

2. P.L. Richards and Q. Hu, "Superconducting components for infrared and millimeter wavelengths," *Proceedings of the IEEE*, 77, 1233-1246, 1989.

3. M. Gurvitch, M.A. Washington, and H.A. Huggins, "High quality Josephson tunnel junctions utilizing thin Aluminum layers," *Appl. Phys. Lett.*, 42, 472-474, 1983.

4. A.W. Lichtenberger, C.P. McClay, R.J. Mattuch, and M.J. Feldman, "Fabrication of Nb/Al-Al_2O_3/Nb junctions with extremely low leakage currents," *IEEE Trans. Magn.*, MAG-25, 1247-1250, 1989.

5. T. Imamura and S. Hasuo, "A sub-micrometer Nb/AlO$_x$/Nb Josephson junction," *J. Appl. Phys.*, 64, 1586-1588, 1988.

6. T. Kasuga, K. Handa, J. Inatani, M. Ishiguro, H. Iwashita, T. Kanzawa, R. Kawabe, K. Miyazawa, Y. Murata, A. Sakamoto, M. Tsuboi, K. Watazawa, K. Yamaji, and M. Yamamoto, "Dual channel all-hard SIS mixer receivers of the Nobeyama millimeter-wave array," *Extended Abstracts of 1987 International Superconductivity Electronics Conference (ISEC '87)*, 99-109, 1987.

7. S. Morohashi and S. Hasuo, "Experimental investigations and analysis for high quality Nb/Al-AlO$_x$/Nb Josephson junctions," *J. Appl. Phys.*, 61, 4835-4849, 1987.

8. H. Kroger, L.N. Smith, and D.W. Jillie, "Selective Niobium anodization process for fabricating Josephson tunnel junctions," *Appl. Phys. Lett.*, 39, 280-282, 1981.

9. S. Morohashi, S. Hasuo, and T. Yamaoka, "Self-aligned contact process for Nb/Al-AlO$_x$/Nb Josephson junctions," *Appl. Phys. Lett.*, 48, 254-256, 1986.

10. A. Shoji, S. Kosaka, F. Shinoki, M. Aoyagi, and H. Hayakawa, "All refractory Josephson tunnel junctions fabricated by reactive ion etching," *IEEE Trans. Magn.*, MAG-19, 827-830, 1983.

11. S. Morohashi, F. Shinoki, A. Shoji, M. Aoyagi, and H. Hayakawa, "High quality Nb/Al-AlO$_x$/Nb Josephson junctions," *Appl. Phys. Lett.*, 46, 1179-1181, 1985.

12. Valpey-Fisher, Hopkinton, MA

13. Dow Corning Corporation, Midland, MI

14. Hoechst Celanese, Somerville, NJ

15. J.X. Przybysz, R.D. Blauer, and J. Buttyan, "Processing techniques for refractory integrated circuits," *IEEE Trans. Magn.*, MAG-25, 1127-1130, 1989.

16. J.H. Kang, D.L. Miller, and J.X. Przybysz, "Fabrication of 12-Bit A/D Converter Using Nb/AlO$_x$/Nb Josephson Junctions," *these proceedings.*

17. H. Hatzakis, B.J. Canavello, and J.M. Shaw, "Single step optical lift-off process," *IBM J. Res. Dev.*, 24, 452-460, 1980.

18. D.R. Winkler, N.G. Ugras, A.H. Worsham, D.E. Prober, N.R. Erickson, and P.F. Goldsmith, "A full-band waveguide SIS receiver with integrated tuning for 75-110 GHz," *these proceedings.*