

Chapter 4

Nanometer-Scale Fabrication Techniques

RICHARD E. HOWARD

Bell Telephone Laboratories
Holmdel, New Jersey

DANIEL E. PROBER

Section of Applied Physics
Yale University
New Haven, Connecticut

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I. INTRODUCTION

In the past thirty years electronic devices based on semiconductors have evolved from a size scale of millimeters to a size scale of micrometers. This thousandfold decrease in size has allowed the development of a vast industry to produce inexpensive integrated circuits, has opened major opportunities for national economic growth, and may start off a new industrial ordering with changes as significant as those of the Industrial Revolution. Even beyond these developments, it is now possible to fabricate patterns $10^{-2} \mu\text{m}$ in size and to see features smaller than $10^{-3} \mu\text{m}$. Under special conditions, individual atoms can be visualized. Thus, further device miniaturization and new device concepts are certain to occur. Since many of the fundamental limits imposed by quantum mechanics and statistical physics will be encountered as devices and structures are made smaller, significant opportunities exist for scientific exploration as well.

This chapter is designed to provide an overview of the new techniques for fabrication at a size scale below 100 nm ($1 \text{ nm} = 10 \text{ \AA}$). A number of nanometer-scale devices and scientific studies have become possible with these techniques, and research in this field has seen a number of recent successes [1].

This chapter is intended for the practicing scientist who may wish to utilize the nanometer-scale techniques, as well as the device engineer who is familiar with current production lithographic techniques. We shall therefore provide some background on the basic lithographic concepts. Our main focus, though, will be on the limits and applications of the nanometer-scale fabrication techniques, not their practicality for current device production. A number of excellent reviews of microlithographic techniques relevant to current production applications are available in this series and elsewhere [2–10], and we draw on these for background material. Most of these reviews treat issues relevant to micrometer-sized structures, down to sizes of $\sim 0.2 \mu\text{m}$. Brief discussions of nanometer-scale fabrication techniques have recently been given [11–13]. Here we shall concentrate specifically on reviewing techniques and studies applicable in the size range below $0.1 \mu\text{m}$. It is in this range that the quantum nature of matter and device performance limits are most readily explored.

II. RESIST PROCESSES AND RESOLUTION LIMITS

A. Resist Processes

With the exception of direct ion-beam processing, current lithographic techniques depend on patterning a layer of a radiation-sensitive material

(resist) [14], such as a polymer, that coats a suitable substrate, as shown in Fig. 1. The incident radiation—electrons, photons, or ions—causes a chemical or structural change in the exposed areas of the resist and leaves them with an etching rate that differs from that of the unexposed areas. The development process removes either the exposed areas (positive tone) or the unexposed areas (negative tone), leaving behind a stencil on the substrate that protects it from subsequent processing. Liquid developers are now standard, though dry (e.g., plasma) development is also possible [14], and can offer specific process advantages.

The patterned substrate is next subjected to either a deposition process, such as evaporation or ion implantation, or an etching process. For etching patterns containing submicrometer-sized features, some form of dry etching, such as ion-beam etching or reactive-ion etching, is usually used to ensure high resolution in the etched pattern. In that case, it is important

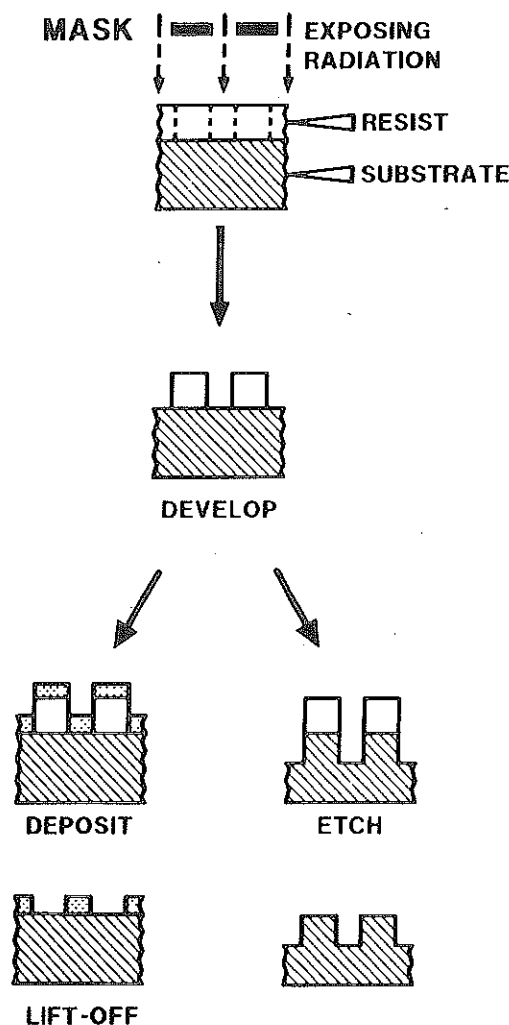


Fig. 1. Schematic of positive resist process showing lift-off and etching.

that the resist be sufficiently resistant to the etching conditions to transfer the pattern to the substrate.

When a resist stencil is used with a deposition process, sections of the substrate are protected by the resist, which is subsequently dissolved away and removed along with the unwanted material. This is referred to as the *lift-off process*. If the deposition is a directional process such as evaporation, the unwanted material is more easily lifted off if the stencil has an undercut profile, as shown in Fig. 2. Nondirectional deposition, such as is obtained with sputtering, is more difficult to use with lift-off processing. (An exception to these considerations would be a selective process such as electroplating, which does not deposit material on the resist. In this case, vertical resist profiles may be desired.) Because good techniques for making undercut stencils are a relatively recent development, lift-off processing has not as yet found much commercial application. Also, for ordinary polymer resists, deposition temperatures cannot exceed $\sim 100^{\circ}\text{C}$, though techniques for using lift-off with high-temperature processes have been demonstrated [15, 16]. The demonstrated high resolution of the lift-off process together with the ability to pattern materials that are difficult to etch has made it important for experimental studies.

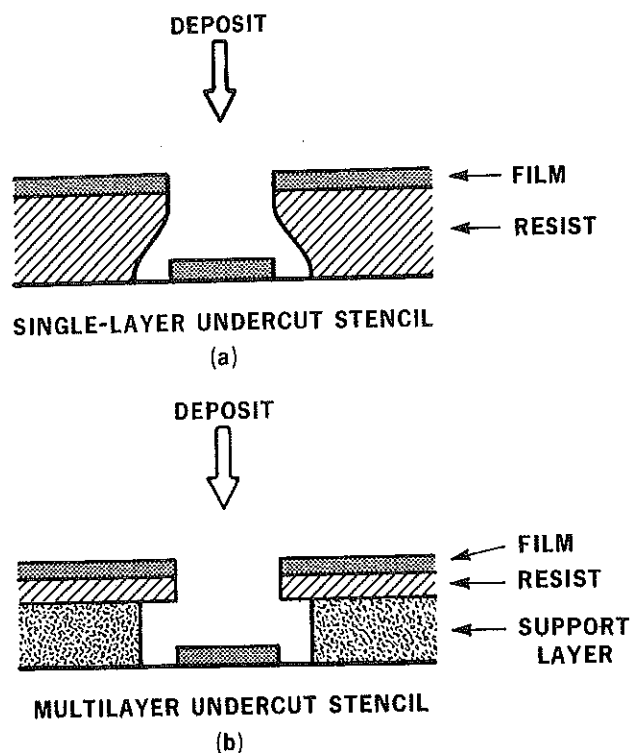


Fig. 2. Application of undercut resist profiles to lift-off.

B. Resolution Limits

For electron, ion, and x-ray exposure, it is often the limitations of the resist itself, not those of the exposure system, that set the ultimate limit on pattern resolution. We shall therefore treat these resist resolution limits before discussing the individual processes of electron, ion, and x-ray exposure. For UV-optical exposure, the resolution is limited by diffraction effects, with resulting dimensions $>0.1 \mu\text{m}$. Of the high-resolution exposure processes, electron exposure and the electron-resist interaction have been the most extensively studied. Also, the exposing beam can be smaller than any known resolution limit. We shall therefore discuss resist exposure in terms of electron exposure.

Table I lists some of the more commonly used resist materials together with their electron-beam sensitivities (required dose for electron-beam exposure) and reported resolutions. Though many materials have been tested as electron-sensitive resists, only two, the polymer poly(methyl methacrylate) (PMMA) and contamination resist, have demonstrated resolutions better than 50 nm and have been used to transfer similar-size patterns to other materials. A resolution of $<50 \text{ nm}$ may be obtainable with other resists on thin substrates or in multilevel configurations (see the following discussion), but these other materials have not been as well studied. When exposure is done on a thick substrate or using a thick resist, the resulting resolution does not necessarily represent an intrinsic lower limit for the resist because electrons scattered in the resist or back

TABLE I

Resist Exposure Characteristics for Electron-Beam Exposure

Electron resist, beam energy ^a	Required exposure dose ($\mu\text{C}/\text{cm}^2$)	Substrate	Smallest resist feature (nm)	Ref. ^b
Contamination, 60 keV	$\sim 10^6$	Thin	2	a
PMMA, 50 keV	500	Thin	16	b
PMMA, 25 keV	50	Thick	<100	c
PSTTF, 20 keV	6	Thick	<100	d
PBS, 25 keV	1	Thick	500	c

^a All exposures are positive tone except contamination and PSTTF. PBS = poly(butene-1-sulfone); PSTTF = polystyrene-tetrathiafulvalene polymer.

^b References:

- a. Zingsheim [17] and Broers *et al.* [18]
- b. Beaumont *et al.* [19] and Broers [20]
- c. Chang *et al.* [10]
- d. Hofer *et al.* [21]

from the substrate can expose the resist in areas adjacent to the incident beam.

PMMA is the most commonly used resist for high-resolution (< 100 nm) studies with all exposure techniques. When it is used as a positive resist, the secondary electrons (with energy $\lesssim 100$ eV) created by the incident radiation break bonds within the polymer, making the PMMA more soluble in a developer such as methyl isobutyl ketone (MIBK). Pore formation due to gas evolution and chemical changes in the resist may also enhance the resist solubility [22]. Their effect on resolution has not been investigated. The effective range for the secondary electrons in PMMA has been estimated to be $\lesssim 10$ nm for electron [20], ion [23], and x-ray [7] exposure; this sets the ultimate limit on the resolution for a resist sensitive to these electrons. At a much larger dose, cross-linking between the polymer chains occurs, and the insoluble residue can be used as a negative resist. Unlike other polymer resists, PMMA shows little tendency to swell during development. Linewidths under 40 nm have been reported for both positive and negative exposures [11, 19, 20, 24–27].

The main disadvantage of PMMA and contamination resist (to be discussed later) is the poor sensitivity (see Table I). As a result of this, PMMA is currently not in general use for the production of devices or masks. As an example of this low sensitivity, consider exposure of PMMA with a high-intensity, 50-keV, field-emission, electron-beam source with a 20-nm-diameter beam of 10^{-7} A [28]. It would take about 1 day to expose a dense pattern on a 4-in. wafer at 20-nm resolution; additional time would be required for stage motion and alignment. The exposure time would be considerably less, but still significant, if only a few fine features were required for each device and if the beam size could readily be varied. Unfortunately, there is an intrinsic conflict between the requirements of high resist resolution and high sensitivity, due to the statistical considerations discussed below.

In addition to exposure sensitivity, a key criterion of resist performance is development contrast. The conventional definition of contrast for positive resist is $\gamma = [\log(D_0/D_i)]^{-1}$, where D_0 is the dose required to effect complete resist removal in a given development time and D_i the (extrapolated) dose at which development just begins. High contrast is important for achieving sharp, nearly vertical, resist edge profiles when the contrast of the exposing process is low. Thus, high contrast is especially important when exposing at linewidths approaching the resolution limit of the exposure process. In general, improved resist contrast results for weaker developers, higher exposures, and larger molecular weight of the initial polymer. Starting polymer molecular weights for PMMA range from 10^5 to 10^6 . PMMA has the highest contrast of widely used resists [7, 29].

The resolution limits due to the polymer size and the development process are not yet clearly established. In the solid form, the polymer is loosely coiled; the size of this starting polymer ball, and thus the initial molecular weight, might be expected to be important in determining the minimum linewidth or minimum edge roughness achievable. A second length scale that may be relevant in determining resolution is associated with the pervaded (dense-packing) volume of the polymer unit after it has been irradiated. To date, there do not appear to be any studies of intrinsic resist resolution that prove that the polymer unit size affects final pattern resolution. Indeed, most high-resolution studies have been done with high molecular weight PMMA. Minimum linewidths achieved in PMMA resists already equal the diameter of the coiled polymer ball, a few tens of nanometers. From the polymer structure one would expect a limiting resolution of roughly this magnitude. The discrepancy between measured and calculated resist edge profiles at this size scale is evidence for such a limitation [19]. Another possible result of the polymer unit size is the loss of adhesion observed for PMMA linewidths < 20 nm [11, 30]. Still, high-resolution metal patterns formed with a PMMA etch mask appear to have an edge definition and smoothness better than 10 nm [28].

Resists that employ atomic-sized units may, at least in principle, be capable of much better resolution than polymer resists. An example of such a material is a contamination resist [31, 32]. It has been known for a long time that an electron beam will decompose thin layers of organic materials, such as vacuum pump oil, and leave behind a "contamination" pattern. This carbonaceous material can serve as a good etch mask for dry processes. Resist features as small as 2 nm [17] and metal lines as fine as 8 nm [18] have been patterned this way. Electron-beam exposure can also cause selective nucleation of vapor-deposited films [17], direct etching of salt films such as NaCl [11, 33], and changes in Langmuir-Blodgett organic films [11, 34]. The exposure mechanisms and the limitations due to secondary electron pathlength are not well understood for these processes. Also, except for contamination resists, transfer of the patterns from the resist into another material has not been extensively studied. For contamination resists, the resolution of the resist formation appears to be set by a length comparable to that of the secondary electron range [31].

In addition to the secondary electron pathlength and the polymer (or resist) unit size, a third limit on the resolution of the resist exposure process is set by the statistical nature of the incident radiation and of the creation of the low-energy secondary electrons that expose the resist. If a minimum resolution area, $A = d_0^2$, is to be exposed in a thin resist, the average number, \bar{n} , of exposing particles (electrons, ions, or photons) incident on that area must be much greater than the statistical fluctuation in

this number, $\sim \bar{n}^{1/2}$ [2, 6, 7]. (Our discussion assumes that the exposing "particles" are emitted in a probabilistic fashion and that no information is extracted regarding the time or direction of emission. This is certainly the case with x-ray photon emission and appears correct for current electron and ion sources, though information on emission could, in principle, be extracted. Also, the criteria for exactly how much \bar{n} should exceed $\bar{n}^{1/2}$ depends on the number of resolution elements exposed and the confidence level required.) Table II lists values of \bar{n} for electron, ion, and x-ray exposure of PMMA, with a value of $d_0 = 10$ nm, which is approximately the minimum resolution limit observed for PMMA [19, 20]. Only ion-beam exposure is in the statistically limited region. Cases where the exposure or development process have only finite contrast have been discussed quantitatively in the literature [2, 6, 7].

Since electrons and x-ray photons interact weakly with typical resists, another statistical limit relevant to the exposure process is the average number of secondary electrons, \bar{n}' , created in a minimum resolution volume of d_0^3 . Using standard energy loss and absorption data [2, 7], we computed \bar{n}' , again for PMMA. For electron [2] and ion exposure, we made the simplifying assumption that all energy dissipated in the resist is converted into secondary electrons of energy 100 eV. For x-ray exposure, the photoelectron energy is close to the x-ray photon energy [2]. (For ion exposure, the dissipation-exposure mechanisms are not yet fully established; also, the secondary electron energy is expected to be lower than

TABLE II
Exposure Statistics for Various Exposure Techniques

Technique, incident energy	Exposure dose ^a	\bar{n} Incident flux in (10 nm) ² area	\bar{n}' Number of exposing (secondary) electrons created in (10 nm) ³ volume	Ref. ^b
Electron beam, 50 keV	5×10^{-4} C/cm ²	3,000	400	a
Ion beam, 55 keV Ga ⁺	1.5×10^{-6} C/cm ²	9	400	b
X ray, 0.28 keV (C _K)				
Moderate dose	500 J/cm ³	2,800	11	c
High dose	10^4 J/cm ³	56,000	220	

^a All exposure data are based on exposures actually used for PMMA resist, with an absorbed energy of order 4×10^3 J/cm³ for electron-beam and for ion-beam exposure.

^b References:

- a. Broers *et al.* [24] and Broers [20]
- b. Seliger *et al.* [35]
- c. Spiller and Feder [7]

TABLE III

Intrinsic Limitations on Resist Resolution

Mechanism limiting resolution	Resulting resolution limit
Secondary-electron pathlength	~ 10 nm
Polymer structure	Not established; probably < 10 nm
Exposure statistics	~ 10 nm (PMMA)
Diffraction (x-ray) and scattering (electron or ion)	Negligible within thin resist layer

that for electron exposure [23]. In any case, ion exposure is not limited by statistical fluctuations in the number of secondary electrons.)

The results of the calculations of \bar{n}' are given in Table II, where it can be seen that only x-ray exposure at a moderate dose (absorbed energy = 500 J/cm^3) may suffer from significant statistical fluctuations. PMMA exhibits a higher contrast at higher x-ray exposure doses [7], and exposures of PMMA with a resolution of ~ 10 nm have indeed been achieved with a high exposure dose of $\sim 10^4 \text{ J/cm}^3$ [36] (see also Section III.D).

It is clear from the data in Table II that in order to achieve a 1-nm resolution element without statistical limitations, one must use a resist that is less sensitive than even PMMA. That resist must also have a very small interaction volume. Resists based on the addition (contamination resist) or removal (salt films) of low-molecular-weight components may fulfill these requirements, though it should be re-emphasized that limits due to secondary electron pathlength are not known for these resists. It will be difficult to achieve 10-nm resolution with resists that are much more sensitive, i.e., that require a much lower exposure dose, than PMMA. Thus, for 10-nm resolution, PMMA appears to be nearly optimum in terms of statistical limits and its exposure sensitivity. For thin resists (< 50 nm thick), scattering or diffraction of the exposing radiation in the resist is not significant compared with the other limitations discussed. We summarize the conclusions on resist resolution limits in Table III.

C. Multilevel Resists

Conventional lithography using a single resist layer is limited by the compromises one must make in choosing the properties of the resist material. Use of a positive resist as an ion etch mask, for example, requires that the same material be extremely sensitive to the exposing radiation yet be stable under bombardment by electrons, photons, and reactive ions in the etching environment. The resist must, in general, also have good con-

trast and high sensitivity to the exposing radiation, adhere well, be suitable for use as an etch or lift-off mask, and leave no residue in the clear areas.

An additional requirement on resist performance is that the resist uniformly coat the substrate. This is straightforward with a flat surface, but after several levels of processing, the substrate can have considerable topographic relief. Under these conditions, a spin-cast resist must be thick to ensure proper coverage. Because of scattering or diffraction effects and the finite contrast of the development process, such a thick resist layer will have reduced resolution and is, in general, not useful for dense submicrometer patterns.

These conflicting requirements can be satisfied by using a resist system containing two or more layers, each of which can be optimized to achieve the desired properties in the final stencil. Often, the lower layers of the composite need not be resists at all; they can be chosen on the basis of desired chemical and physical properties. Table IV summarizes some examples of processes developed to date and indicates some of their special features. Reviews of multilevel resist techniques have recently been given by Moran [37] and by Hatzakis [38].

Much of the initial interest in multilevel resists originated from the need to produce undercut profiles for use with lift-off processing [39]. Later work emphasized the utility of a vertical resist profile as an etch mask and

TABLE IV
Examples of Multilevel Resist Techniques

Technique	Resist system ^a	Special features	Refs ^b
Optical	PR-thin Al-PR	Large undercut achievable	a
	Chemically hardened PR	Simple; single resist layer	b
	PR-SiO ₂ -polymer	General; vertical profiles	c
	PR-PMMA	PR acts as deep-UV mask	d
Electron beam	Copolymer-PMMA	Mutually exclusive developers	e
	PMMA-copolymer	More sensitive lower layer	f
	PMMA-Ge-copolymer	25 nm resolution, thick substrate	f

^a The top layer of the multilevel is listed first. PR = photoresist; copolymer = copolymer of methylmethacrylate and methacrylic acid P(MMA-MAA).

^b References:

- a. Dunkleberger [47] and Dolan [104]
- b. Hatzakis *et al.* [43]
- c. Moran and Maydan [40]
- d. Lin *et al.* [52]
- e. Hatzakis [51] and Haller *et al.* [50]
- f. Howard *et al.* [26]

the advantages of a thick stencil for obtaining step coverage [40]. Finally, recent work has demonstrated that multilevel resists can be used to make both simple patterns and complex, self-aligned devices with dimensions below 100 nm [25, 41, 42].

Though it is possible to obtain an undercut profile in a single layer of resist (Fig. 2a), the techniques currently available have not demonstrated resolutions below 100 nm. Chemical hardening of the surface of an optical resist before development can leave an overhang in the final profile [43]. This process, like optical back-projection exposure through a transparent substrate [44], is limited in resolution to a few hundred nanometers by diffraction effects. Undercut profiles also occur in electron-beam exposure of thick resists because electron scattering effects increase the dose at the bottom of the resist [45, 46]. These same scattering effects reduce the contrast of the exposure and limit resolution for a thick resist to a few hundred nanometers.

The general multilevel resist scheme is shown in Fig. 2b. A thin layer of resist is separated from the substrate by a thicker layer of material (usually polymer), which will form the support layer for the stencil after processing. If the two layers cannot be directly deposited on top of each other, e.g., because of interdiffusion during spin casting or because better control over processing of the support layer is necessary, an intermediate layer can be used for separation. Examples of intermediate layers are metals [47], semiconductors [26, 27, 48], oxides [40], or even plasma-hardened polymers [49].

After patterning the upper layer using one of the exposure techniques to be discussed in Section III, the intermediate layer, if present, is etched using the upper layer as a mask. The pattern is then transferred to the lower layer using the upper (or intermediate) layer as a stencil. If an undercut is desired, an etch with an isotropic component, such as a plasma or wet etch, can be used. It is also possible to get a well-controlled undercut profile by using a resist for both the lower and upper layers. In the case of positive tone, if the lower layer is pre-exposed [47] or is more sensitive than the upper layer [25, 50], or if it can be processed with a developer that does not affect the upper layer [51], the increased linewidth in the lower layer provides the undercut. Vertical walls can be obtained by using the upper (or intermediate) layer as a mask for deep UV [52] or x-ray [52a] exposure of the lower resist layer. Alternatively, an inorganic intermediate layer can be used as a mask for anisotropic reactive-ion etching of the lower layer. Since etch ratios between polymers and inorganic materials can be large, this etching technique leads to high-aspect-ratio profiles in the polymer support layer [26, 37, 40, 52b]. A controlled undercut may then be formed using an isotropic etch.

Figure 3 shows an example of a three-level resist processing sequence for a system that has demonstrated linewidths as small as 25 nm using electron-beam lithography on thick silicon substrates [26, 27]. Figure 3a shows the thin (100 nm) layer of PMMA above a thicker layer (280 nm) of a copolymer of methylmethacrylate and methacrylic acid. The two layers are separated by a 25-nm-thick layer of thermally evaporated germanium. After exposure and development of the PMMA (Fig. 3b), the resulting stencil is used as a mask for reactive-ion etching of the germanium layer (Fig. 3c). Since germanium etches very slowly in an oxygen plasma, it can be used as a mask for anisotropic reactive-ion etching of the thick lower polymer layer (Fig. 3d); the resulting structure has the resolution of the thin PMMA resist layer but sufficient thickness for use as a lift-off stencil.

As various multilevel resist processes were developed, it was noted that increased resolution for both optical and electron-beam exposure was a by-product of the technique [25, 40, 52]. For optical exposures, standing-wave effects from reflections off the substrate can be eliminated by using an absorbing lower layer [52b]. For electron exposure, use of a thin resist spaced above the substrate can reduce effects due to electron scattering in the resist or back from the substrate [53]. These electron-scattering effects are significant in high-resolution lithography and will be discussed in more detail in the electron-beam exposure section. An additional advantage of multilayer resists, one that is very important for high-resolution lithography, is the increased control of development parameters relative to single-layer resists. Since no known resist has infinite contrast and since all exposure techniques have some scattering or diffraction effects, the width of the exposed areas will continue to grow with development time (for positive-tone resists). Thus, for a thick layer of re-

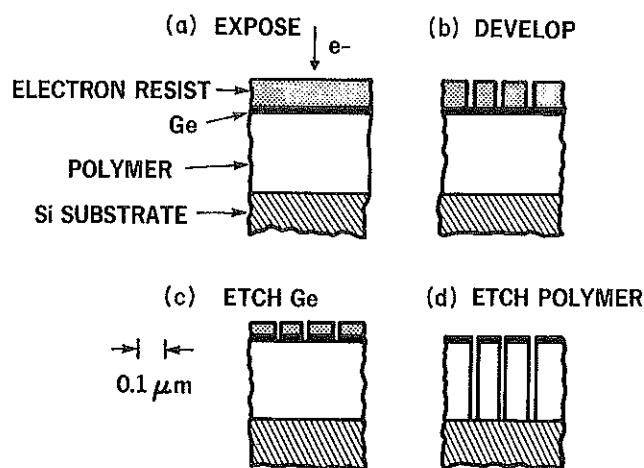


Fig. 3. Trilevel resist stencil preparation. (From Howard *et al.* [26].)

sist, the top of the pattern will be significantly overdeveloped in the time necessary to clear all of the resist to the substrate. In a multilevel process, the thin upper layer need only be developed long enough to clear to the intermediate or support layer; the rest of the stencil is cleared using a process having little or no development effect on the upper resist. Thus, thin resist is necessary for high resolution, and multilevel techniques can be used to fabricate useful stencils from these thin resist layers. Examples of results obtained with multilevel resists will be presented in Section III.

III. EXPOSURE AND PATTERNING TECHNIQUES

For exposure of the resist, parallel or serial methods may be employed. Parallel exposure, as exemplified by whole-wafer ultraviolet exposure with a contact mask, offers high throughput but does not allow local alignment or correction for vertical or in-plane wafer distortion. Fully serial methods, exemplified by electron-beam raster-scan exposure, allow alignment, focusing, and correction for wafer distortion. Beam intensity can also be controlled to compensate for proximity effects (see Section III.A). Currently, however, throughput is not adequate for general production. A combination of these methods, such as step-and-repeat optical exposure of individual chips on a wafer, can combine the advantages of the serial and parallel methods.

It is useful to keep in mind for the future that current refractive optical lenses [8] and electron-optical systems [11, 13] have on the order of $\sim 10^8$ resolvable spots within the image field. Thus it is clear that in addition to system resolution, accuracy of alignment and pattern joining will be increasingly important for VLSI and beyond. Here, however, we shall deal with fundamental resolution limits and techniques for achieving these limits.

We shall not discuss optical lithography, which has a resolution limited by diffraction. Features as small as $0.2\text{ }\mu\text{m}$ have been produced in laboratory studies [44] with a large-numerical-aperture, small-image-field projection system based on a high-quality optical microscope. Linewidths of 0.4 to $0.8\text{ }\mu\text{m}$ may be expected for complex patterns produced with future optical projection systems [8, 13]. The use of resists with improved contrast or shorter optical wavelengths could somewhat reduce this limiting linewidth. Still, dense patterns with linewidths under $0.1\text{ }\mu\text{m}$ cannot be expected with exposing radiation wavelengths greater than $0.2\text{ }\mu\text{m}$.

The emerging technologies of projection and proximity printing with electrons will also not be discussed. These processes have not yet demon-

strated resolutions better than $0.1\ \mu\text{m}$ but may do so in the future as the masks and exposure systems are improved. Reviews of this field have recently been given [5, 54].

A. Electron-Beam Writing

Electron-beam lithography is the best developed and most versatile high-resolution pattern-generation technique now available. Excellent discussions of the basic principles, available equipment, and commercial importance are available in this series and elsewhere [2, 5, 5a, 6, 9, 10]. In this section, we shall discuss only the application of electron-beam lithography in fabricating features smaller than 100 nm and the limitations of the process as currently perceived.

Though electron beams smaller than 1 nm can be formed and accurately directed with digital or analog techniques, there are a variety of processes that degrade resolution and cause the minimum linewidth to be much greater than 1 nm. The lower size limit to the electron-beam exposure process must be the size of the volume sampled by an *incident* electron during an inelastic interaction with the resist. (Fundamental considerations appear to prohibit exposing resists using only elastic interactions between electrons and the resist.) From resolution studies using a scanning transmission electron microscope (STEM), the inelastic interaction volume seems to be about 1.5 nm in diameter [55]. None of the present advanced techniques approaches this resolution for transferring a pattern to a "device" film. Patterning at this nearly atomic size scale will have to be the topic of a future review.

The resolution achieved in many electron-beam exposure studies has been limited by the scattering of the incident electrons in the resist or from the substrate. Forward scattering in the resist layer can be an important limitation, but it is easily made negligible by using high beam voltages and thin ($<100\ \text{nm}$) resists [20]. Resist layers this thin can only be used effectively for pattern formation if they are incorporated in a multilevel resist scheme or, if used directly, for patterning very thin films.

Although forward scattering in the resist can be made negligible, a further limitation results because of the long range of the primary electrons. A flux of backscattered electrons will be generated from an average depth of several micrometers in the substrate and, thus, can be expected to give a diffuse exposure over an area several micrometers on a side. For typical micrometer-sized patterns of current commercial interest, this causes a "proximity effect" between the exposures of adjacent features [56].

For high-resolution ($<0.1\ \mu\text{m}$) patterns in thin resists, the backscat-

tered electrons from the substrate will only add an average background exposure because they are spread over a large area compared with the 100-nm features. Broers [20] has used measured values of the factor for backscattered electron exposure to calculate that this background scattering should limit exposure contrast for thin resist to a maximum of about 50% for dense electron-beam exposures with linewidths between 50 nm and 2 μm on thick silicon substrates (see Fig. 4). Broers also calculated the intrinsic resist contrast in the absence of exposure by backscattered electrons. This is denoted in Fig. 4 as the case of thin resist on a thin substrate. In this case, only the limits observed in exposures on membrane substrates, attributed to secondary electron pathlength, were considered. Note also in Fig. 4 the surprising conclusion that optical-projection exposure can achieve better contrast than electron-beam exposure of 1- μm thick resist for linewidths between 0.3 and 6 μm , due to electron scattering in the resist and back from the substrate (Fig. 5a).

Figures 5b and 5c illustrate a technique for avoiding the effects of backscattered electrons by eliminating the bulk of the substrate. With thin (<100 nm) membranes of a low atomic number material, like Si_3N_4 [31, 32] or carbon [18, 19], electron backscattering can be essentially eliminated. Figures 5b and 5c show, respectively, the case of such a membrane, typically 60 nm thick, being used with a contamination resist or a thin layer of PMMA. With the contamination resist, resist lines finer than

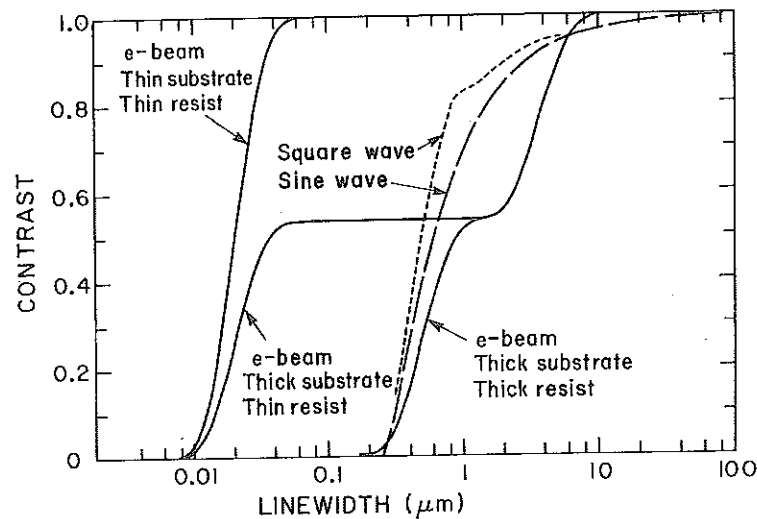


Fig. 4. Contrast versus linewidth for electron-beam and optical-projection exposure. Curves shown are for electron exposure of patterns of equal lines and spaces in thin PMMA on a thin (membrane) substrate, in thin PMMA on a thick Si substrate, and in 1- μm -thick PMMA on a thick Si substrate (beam energy = 20 keV). Also shown are optical projections of a sinusoidal (broken line) and square-wave (dashed line) mask with an objective numerical aperture of 0.41. (From Broers [13], © 1980, IEEE.)

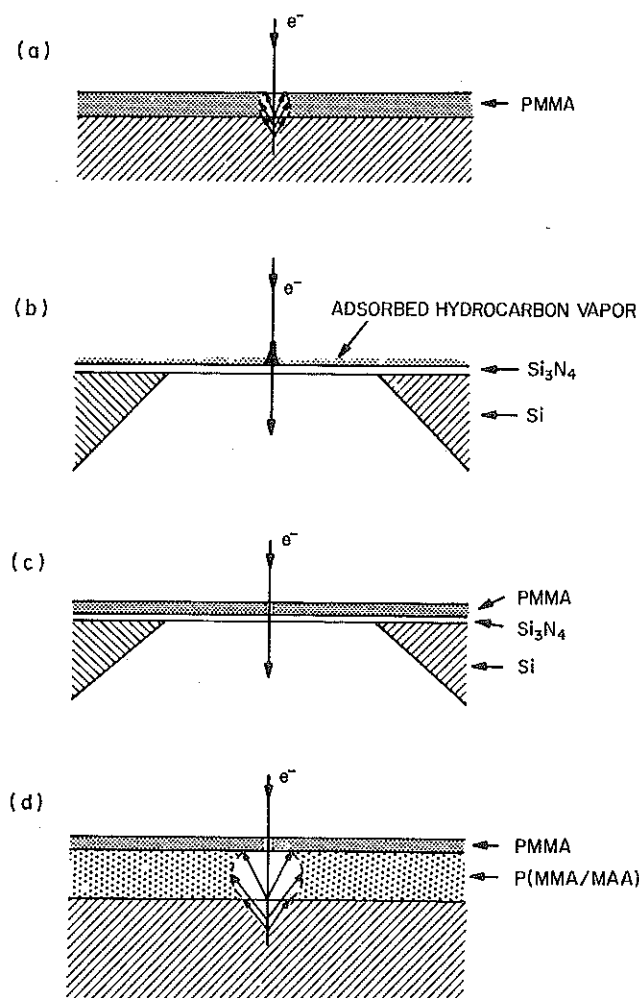


Fig. 5. Electron-beam exposure showing scattering and methods to reduce scattering. (a) Thick resist; (b) contamination-resist lithography on a membrane; (c) polymer resist on a membrane; (d) high-resolution two-layer resist. (From Howard [12].)

2 nm have been made [17]. Metal patterns as fine as 8 nm have been produced by ion etching using the contamination resist as a mask [18]. Such lines are shown in Fig. 6. Very careful process control is required to achieve 8-nm linewidths; somewhat larger lines, 25–70 nm wide, are more readily produced and have been used to make superconducting microbridge devices in ion-etched Nb films [32, 57].

Using PMMA on a Si_3N_4 membrane, dense patterns with lines as fine as 25 nm were formed in metal by ion etching using the PMMA as an etch mask [24]. These results are shown in Fig. 7. PMMA lift-off patterns as narrow as 16 nm have been made on carbon membranes [19]. Finally, electron beams have been used to etch lines as narrow as 1.5 nm and

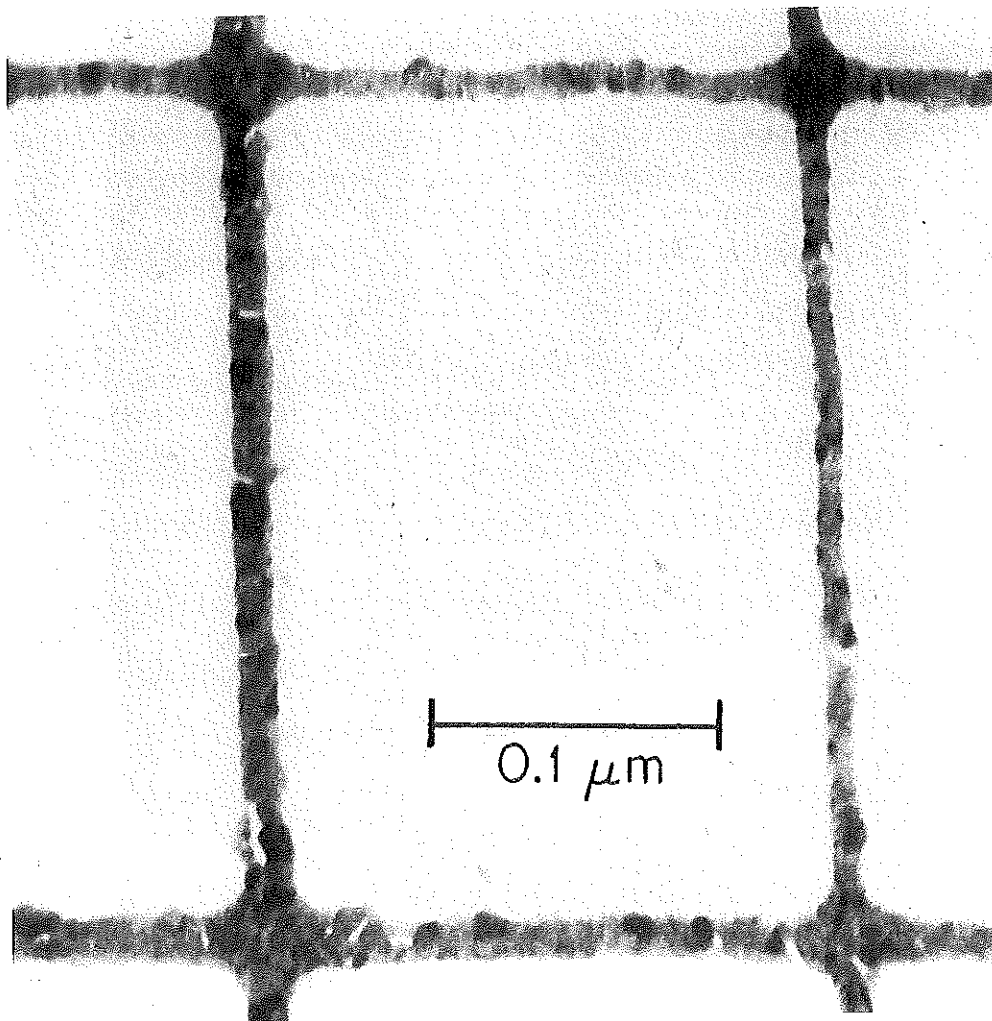


Fig. 6. Bright-field scanning transmission electron micrograph of Au-Pd lines patterned by ion etching with a contamination-resist mask (Fig. 5b) on a carbon membrane. Smallest lines are 8 nm. (From Broers *et al.* [18].)

holes as small as 2 nm in diameter into NaCl films by directly vaporizing the material [33].

These experiments on membranes using PMMA were all performed in STEM machines having electron beams much smaller than the achieved linewidth. Resolution was limited by effects within the resist or by development processes. The results obtained on Si_3N_4 membranes were interpreted to give a measure of the effective range, ~ 12.5 nm, for the secondary electrons responsible for exposing the resist [20]. (Secondary electrons with a broad spectrum of energies are created [57a]. A more detailed calculation of the secondary electron exposure would thus be desir-

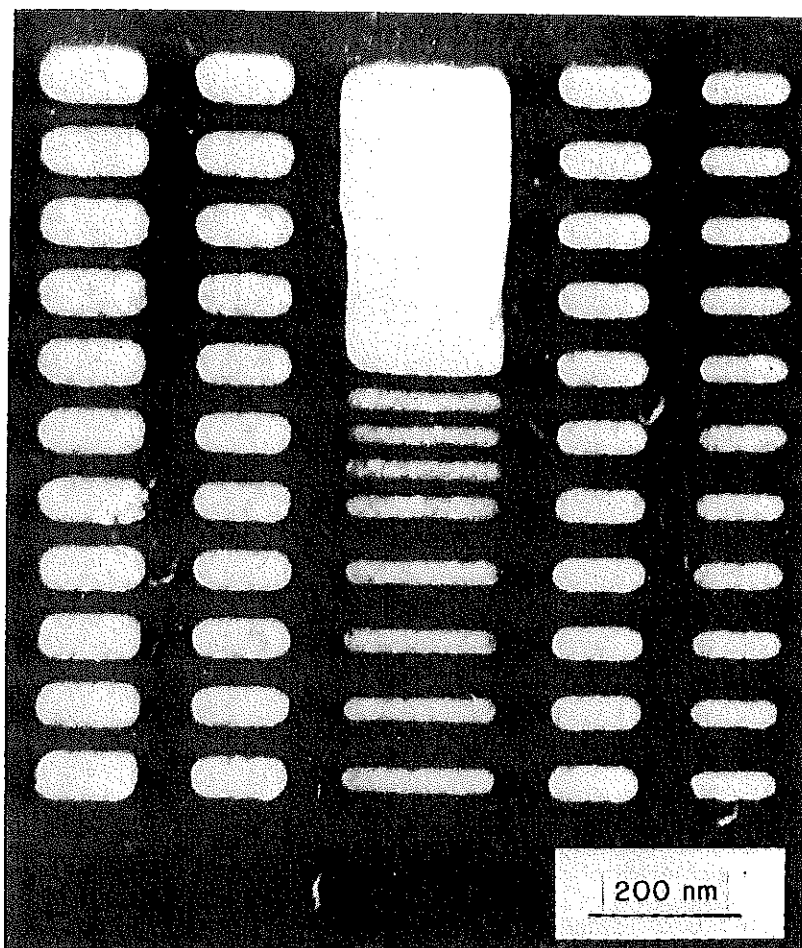


Fig. 7. Bright-field scanning transmission electron micrograph of Au-Pd pattern produced by ion etching with a PMMA resist mask on a Si₃N₄ membrane (Fig. 5c). Smallest lines and spaces are 25 nm. (From Broers *et al.* [24].)

able.) In other work on a carbon membrane, a detailed analysis of the resist edge profile was given [19]. All predicted profiles were vertical, whereas the experimental profiles were all sloping and "overcut" (the opposite of the profile shown in Fig. 2a). In making the predictions, it was assumed that the only important factor determining the resolution of the exposure and development process was the finite range of the secondary electrons. Also, bulk resist development rates were used. As was noted in the section on resists, at this size scale, additional factors, including both the mechanics of development (solvent gradients, polymer uncoiling, etc.) and the polymer "grain size," must be included for a complete description of the exposure-development process. Data on these other effects are not yet available. Thus, at present, the ultimate resolution limits in polymer resists are not established with certainty. Even so, linewidths

of ~ 20 nm are now achievable. At these dimensions, the resolution limits appear to be due to the resist.

The studies on membrane substrates have been invaluable for studying questions of ultimate limits in the resist process; they also facilitate detailed analysis of the results using standard transmission electron microscopy techniques. Unfortunately, other than making single-layer devices from deposited films like the superconducting microbridges, direct applications of these membranes seem limited. At the cost of increased complexity, membranes might be used to fabricate masks for use with printing techniques, such as x-ray lithography (to be discussed later). However, the wide variety of phenomena at size scales below 100 nm would be most easily studied if the resolution and flexibility of electron-beam lithography were directly available on bulk substrates.

With thick substrates, reduced contrast results from the scattered electrons (see Fig. 4) and makes it difficult to obtain < 100 -nm sized patterns in a single thick layer of resist. Multilevel resist techniques, in contrast, have been used to make useful stencils as small as 25 nm wide on thick silicon substrates [26, 41]. The use of a thin, upper resist layer minimizes forward scattering effects, and the bilevel (Fig. 5d) and trilevel (Fig. 3) techniques compensate for reduced contrast by giving better control over development parameters, as discussed in the section on multilevel resists. Some additional resolution improvement in the multilevel process may be due to a reduction in the exposure by backscattered electrons because of the presence of the lower layer. However, detailed simulations of this have not yet been done for the high-resolution resist systems.

A comparison of all the high-resolution studies done with electron-beam lithography indicates increasing difficulty in producing features much smaller than about 20 nm. Since all of these studies were done using PMMA and all the limits look similar, it is important to investigate another resist material, such as PSTTF [21], to separate materials effects from more fundamental limitations such as secondary electron exposure. Still, resolutions of ~ 25 nm are achievable for dense patterns, and for isolated features, 10 nm linewidths can be achieved, at least for specific materials.

B. Ion-Beam Writing

Two of the major problems of electron-beam lithography, resist exposure sensitivity and exposure by backscattered electrons, can be reduced by using a heavier particle, such as an ion, to do the exposure. Since ions have a much larger cross section for the production of secondary elec-

trons than an electron of equivalent energy [2], they lose energy more rapidly along their pathlengths. Thus, the sensitivity of the resist to ion exposure is much greater than for electron exposure (see Table II). In addition, the average energy of the secondary electrons generated by ion exposure is smaller than that of the secondary electrons generated by an incident electron beam [23]. Thus, resolution limits arising from the secondary electron range as well as from proximity effects from backscattering of the primary beam from the substrate will be smaller for ion-beam lithography.

The main obstacle to developing ion-beam lithography has been the absence of appropriate sources. Recently, field-ionization [58] and liquid-metal sources [59] have been developed with brightnesses similar to those available from thermal electron sources. Using a column similar to that of an electron-beam lithography system, a focused ion beam with a diameter below 100 nm has been produced. Using a 55-keV Ga^+ beam, thin layers of PMMA have been exposed and the developed stencils used as a mask for the ion etching of a gold film. Features as fine as 40 nm were formed. A dose of only about $1.5 \times 10^{-6} \text{ C/cm}^2$ was required—a factor of ~ 300 smaller than an equivalent high-dose electron-beam exposure [20]. The development of high-speed deflection systems together with these high-brightness sources could lead to this process becoming an important alternative to electron-beam lithography. Ion-ion interactions and chromatic aberration from the large energy spread of the source may limit the minimum spot size to tens of nanometers, which is much larger than the minimum for electron beams but still small enough to be competitive for most applications.

A potentially important alternative technique is to use the ions to process a substrate directly rather than to expose the resist. Localized doping, sputtering, or even heating can be performed. Seliger *et al.* [35] used a Ga^+ beam to do direct ion-beam etching of a gold film and achieved an etched linewidth of 38 nm. Localized ion implantation of silicon was also demonstrated. Subsequent work has included fabrication of a GaAs FET with all of the active areas defined using focused-ion-beam implantation [60]. Though far too slow for standard wafer processing, these techniques may be important for custom fabrication of small circuits and devices or for repair of integrated circuits.

C. Ion Printing

The same advantages of resist speed and resolution that are offered by ion-beam writing can also be obtained with ion-beam printing. Sources

with a relatively high flux of collimated ions can readily be produced. Unlike x rays, collimated ion beams can be focused, making possible projection [61] as well as proximity printing. The practical application of this lithography requires a suitable mask technology; with this, ion printing should prove a strong competitor to x-ray printing.

Because of the large fluxes available, large-area ion beams are not limited to exposing resists. For example, ion implantation is a common technique. It can have lateral resolution of less than 100 nm when an absorbing mask, usually a resist or SiO_2 , is used directly on the surface of the sample. A less well known process uses ion-induced damage to increase the etch rate of a material other than a conventional resist. Though this requires much larger doses than for exposing a polymer resist, it is easily implemented using available sources. A variety of materials including [61] Si, SiO_2 , Si_3N_4 , Ni, Mo, and even LiNbO_3 [62] have been patterned this way. Direct ion etching is, of course, a widely used technique and is discussed in Section III.E.

In principle, masks for ion printing should be similar to those used in x-ray lithography, but the short range of ions in even very low atomic number materials complicates the problem considerably. The resolution of the exposure process itself in a conventional resist has been demonstrated by using gold patterns directly deposited on thin layers of PMMA. Resist lines 40 nm wide were exposed using H^+ ion exposure through such a thin "contact" mask [63]. A closely related technique is to use a freestanding mask with the pattern defined by completely open areas [64, 65]. Though edge definition below 100 nm has been demonstrated for proximity prints with H^+ [63] and Li^+ [65] ions, the application of such masks is hampered by the geometrical restrictions inherent in an open mask.

Other current candidates for masks are based on absorber layers deposited on a membrane. Because of the high rate of energy loss of ions in matter, only a thin absorbing layer is needed for defining the pattern. Unfortunately, a membrane of an amorphous material must be very thin (~ 100 nm), posing a potential stability problem even greater than that for x-ray lithography. An alternative for the mask support membrane is to use a single-crystal material, such as Si, in which the ions can travel by channeling [64, 66]. Much thicker (700-nm to 6- μm) membranes can be used, leading to a more robust mask. In addition, the absorbing layer on such a mask can be thinner since it need not absorb the ions, just deflect them sufficiently to reduce channeling. However, scattering in such a channeling membrane is still enough that proximity printing cannot be used for linewidths below 0.1 μm . Thus, ion printing may become important for fabrication above 100 nm, but further improvement in the mask

technology is necessary to take full advantage of the inherent resolution of the ion-exposure process.

D. X-Ray Printing

X-ray lithography uses photons of wavelengths from 0.4 to ~ 5 nm and can achieve a resolution of ~ 20 nm [30], approaching that of electron-beam lithography and an order-of-magnitude better than that of optical [44] or deep-UV lithography [8]. Excellent general reviews of x-ray lithography have been given [2, 3, 7], as well as discussions of the production applicability [67, 68] and of resists [69]. We shall emphasize here the aspects of x-ray lithography that relate to ultimate resolution limits and methods of mask production for approaching these limits.

Sources of soft x rays use electron bombardment of a fixed or a rotating target, hot plasmas, or electron storage rings, in order of increasing x-ray photon flux. The first two classes of sources produce characteristic x rays from electronic transitions of excited atoms. The electron storage ring may ultimately be preferred for device production because of its brightness and also because of the beam collimation and nonmonochromatic x-ray spectrum [68]. For laboratory studies, electron bombardment of a fixed target is readily accomplished [70].

In x-ray lithography, exposure takes place by absorption of x-ray photons and production of photoelectrons that can cause chain scission or cross-linking. Because of this, electron-sensitive resists can also be used as x-ray resists. X rays in the shorter wavelength region, 0.4–0.7 nm, are more weakly absorbed, thus allowing thicker mask substrates and transmission of the radiation out through vacuum windows. However, mask absorbers must be thicker, and the intrinsic resolution is only ~ 100 nm because of the fairly large range of the photoelectrons. The longer wavelength x rays can achieve much better resolution but require thin mask substrates and a vacuum environment. A listing of some of the characteristic x-ray lines used for exposure and information on their interaction with polymer resists is given in Table V.

The resolution of the x-ray exposure process for intimate contact between the mask and the substrate is determined by three factors: (1) the pathlength of the photoelectrons in the resist, (2) the diffraction effects of the x rays, and (3) the intrinsic resolution of the resist. (In contrast to the cases of electron and ion exposure, there is no scattering of the primary "particles" in the resist or mask, or from the substrate.) For intimate contact between a thin mask and thin resist, the minimum linewidth due to diffraction alone is set by the wavelength λ of the exposing radiation. However, practical masks and resist layers are not thin compared with

TABLE V
Characteristic X-Ray Lines^a

Source	Energy (keV)	Wavelength (nm)	Secondary-electron pathlength (nm)
Rh _L	2.7	0.46	65
Al _K	1.5	0.83	35
C _K	0.28	4.5	5

^a Data are from Spiller and Feder [7].

the wavelength, so that the wavelength of the exposing radiation is certainly a lower limit on linewidth broadening due to diffraction.

When the mask is not in intimate contact with the resist and for finite resist thickness, significant diffraction effects can be evident, as well as penumbral effects due to the finite size of the x-ray source. With a mask-resist separation of S , the minimum linewidth W_{\min} that can be replicated in thin resist, as determined by diffraction, is given approximately by [13]

$$W_{\min} \approx (\lambda S)^{1/2}$$

for $S \gg \lambda$. With resist thicknesses comparable to S , this minimum linewidth is achieved only at the surface of the resist; the exposure linewidth is greater at the resist-substrate interface. Thus, it is difficult to make very narrow lines in a thick resist layer using x-ray exposure.

Shorter wavelengths encounter reduced diffraction effects, whether for intimate contact (conformal) printing or for proximity printing (mask and substrate separated). However, a shorter wavelength will result in a higher photoelectron energy and a longer photoelectron pathlength. Data on the photoelectron pathlength from Spiller and Feder [7] are given in Table V. The combined resolution limit for diffraction ($\geq \lambda$) and photoelectron pathlength is seen to be minimized for $\lambda \sim 5$ nm, for which a minimum resolution of ~ 10 nm may be expected. Indeed, Feder and co-workers have used a melanin granule from a frog retina cell as a mask to replicate its structure into PMMA with a resolution < 10 nm [36]. The source was a synchrotron, producing x rays between 3.0 and 4.4 nm. The PMMA layer was not fully developed; the partially developed topography was viewed with a high-resolution reflecting SEM. For x-ray line sources, C_K radiation with $\lambda = 4.5$ nm is optimal for high-resolution work, and the smallest fully developed patterns have been produced using C_K radiation and edge-defined masks [30]. Isolated resist line patterns as narrow as 15 nm were produced in PMMA, and a metal line 20 nm wide was produced by lift-off of a 60-nm-thick layer of PMMA.

X-ray masks for contact printing consist of a thin membrane substrate on which an x-ray absorber is patterned. The $\sim 1\text{-}\mu\text{m}$ -thick substrate must have significant transmittance; for shorter wavelengths, Si and various compounds of low atomic number are satisfactory. For C_K radiation, substrates consisting largely of carbon, such as polyimide, are required. The absorber is a high atomic number material, typically gold, fabricated by the standard techniques of ion etching, lift-off, or electroplating. Electron-beam lithography is usually used to define the original mask-absorber pattern.

Absorber patterns with the smallest linewidths and very high aspect ratio can be most easily fabricated by a shadowing technique [30, 70, 71]. In Fig. 8 we show a mask made with this technique; the absorber is evaporated at an angle to the substrate, as shown, and the edge of a step in the substrate defines the absorber pattern. The linewidth of the absorber pattern is determined by the film thickness and thus can be extremely small. Although only simple mask patterns are possible with such a shadowing technique, these edge-defined masks have been an excellent vehicle for testing lithographic resolution. Edge-defined mask patterns for cer-

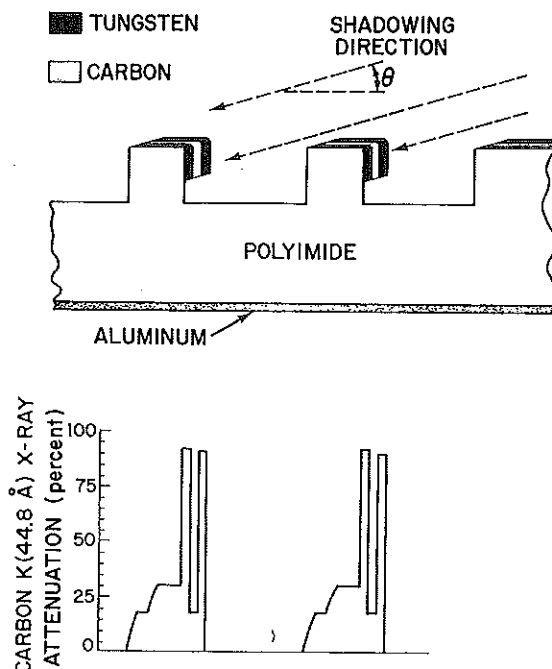


Fig. 8. High-aspect-ratio x-ray absorber mask produced by shadowing. The structure in polyimide was replicated from a SiO_2 pattern produced by holographic exposure and reactive-ion etching. In the calculation of attenuation, the uniform attenuation of the polyimide membrane is not included. (From Flanders [30].)

tain two-dimensional structures are also possible at the same size scale [72, 73].

To replicate patterns with 20-nm resolution, intimate contact between mask and resist is required. Electrostatic hold-down of a conformal mask has proven successful [70]. Such conformal mask techniques, although useful for devices that can be patterned with a single exposure, are not likely to be adopted for large-scale production of semiconductor devices. Most production environments require significant mask-to-substrate spacings of, say, 40 μm , [74] and shorter x-ray wavelengths. However, for laboratory studies of single-exposure or self-aligned device structures, the full resolution of x-ray lithography can already be utilized.

In Tables VI and VII we summarize the discussion to this point. Table VI lists some of the factors that currently limit the resolution in conventional (i.e., production-oriented) exposure systems and some of the solutions previously discussed for improving the resolution. Although many of these solutions cannot be used in production systems, they can be utilized in laboratory studies. Table VII presents results that represent the current state of the art for achieving high resolution in laboratory studies with the various patterning techniques treated here. The different entries have already been discussed. Special exposure systems, masks, or resist techniques were necessary to achieve these results; even so, they demonstrate dramatically the inherent capabilities of the various resist and exposure methods.

TABLE VI
Factors Limiting Resolution of Conventional Exposure Systems

Exposure method	Factors limiting resolution ^a	Solution
Electron beam	Forward scattering in thick resist	Thin resist
	Backscattering from thick substrate	Multilevel resist or membrane substrate
Ion	Forward scattering in thick resist	Thin resist
	Scattering in mask support membrane (if printing)	Thin membrane; intimate mask-substrate contact
	Beam diameter	—
X-ray	Diffraction; finite source size	Intimate mask-substrate contact
	Mask not fully opaque	Edge-defined mask (if appropriate)

^a Factors listed here limit the resolution of current systems that are intended for production applications.

TABLE VII

Final Pattern Resolution Achieved with Various Patterning Techniques^a

Exposure technique	Resist and process	Resolution achieved (nm)	Refs. ^b
Electron beam			
Thick substrate	PMMA lift-off	100	a
	PMMA trilevel resist lift-off	25	b
Thin substrate	PMMA lift-off	16	c
	PMMA ion-etch mask	25 ^c	d
	Contamination-resist ion-etch mask	8	e
Ion beam	PMMA ion-etch mask	40 ^d	f
	Direct ion etching	38 ^d	f
X ray	PMMA lift-off	20	g

^a We consider here patterns *transferred* from the resist to another film, which, in all cases, was a thin metal film. Positive exposure of a single layer of PMMA resist was used, unless noted. Ion-beam and x-ray exposures were on thick substrates.

^b References:

- a. Sedgwick *et al.* [75]
- b. Howard *et al.* [26]
- c. Beaumont *et al.* [19]
- d. Broers *et al.* [24]
- e. Broers *et al.* [18]
- f. Seliger *et al.* [35]
- g. Flanders [30]

^c Dense line patterns.

^d Lower size limit probably determined by exposing beam size.

E. Etching

The most common patterning technique for current device production is wet chemical etching. It has the advantages of being simple and almost universally applicable. In addition, it is often possible to develop processes with a very high degree of selectivity with respect to composition or even crystal structure. These advantages are outweighed in high-resolution applications by the isotropic nature of wet etching in all but single-crystal materials. The undercutting of masking layers makes it difficult to control the dimensions of features that are of the same size as the etch depth. Also, in most applications, film thicknesses cannot shrink in proportion to linewidth, or line resistances and current densities would be excessive. Thus, as circuits shrink, they begin to look less planar and more like three-dimensional "high-rise" structures that cannot be fabricated using simple isotropic etching techniques. Better control of wet etching

can be achieved by using orientation-dependent etches in single-crystal materials, as is done for V-MOS transistors, but this approach has not been extended to features smaller than 100 nm and is not a general technique.

Wet etching has seen an important application in ultra-high-resolution studies, however, for the fabrication of thin (≥ 60 nm) membranes of Si, SiO₂, or Si₃N₄, using the selectivity of an etch to define a vertical dimension [75, 76]. Such structures have been used as tunneling barriers for superconducting devices [76] and have played an important role as membrane substrates for high-resolution electron-beam lithography, as discussed earlier [31].

The selective etching of an exposed resist is a second example of a high-resolution chemical etching process. The resolution and selectivity are high enough that three-dimensional structures with minimum dimensions smaller than 20 nm can be made (see the section on x-ray printing for examples). Although limits due to effects of diffusion in liquids must become important at some scale, they do not seem to be a major limitation for current processes (e.g., high-resolution, liquid-developed multilevel resists [25].) It is also not known at what size scale it will no longer be appropriate to use etch rates derived for bulk samples; presumably, for resists the polymer-ball size (tens of nanometers) will determine this size limit.

With the exception of samples containing good etch stops (discussed previously), most high-resolution etching is done using some type of dry processing in which beakers of chemicals are replaced by vacuum systems full of ions and free radicals [77, 78]. These techniques can reduce undercutting as well as eliminate effects such as resist swelling that degrade resolution in wet processing.

The first dry etching processes studied were sputter etching and ion-beam etching with inert gas ions. Both depend on bombarding a surface with ions such as Ar that locally eject atoms of the substrate. Since this is a mechanical, not chemical, process, it is not possible to obtain selectivity as high as in a wet etch; selectivity factors of 10, though, are possible between some materials [79]. Redeposition of the ejected material and artifacts due to reflected ions (trenching) limit the geometry and resolution of the final pattern. For shallow etching, the resolution is limited by the size of the interaction between the incident particle and the substrate material. An upper limit on this dimension is given by the successful Ar ion-beam etching of 8-nm-wide Au-Pd lines that were masked by a contamination resist pattern (see Fig. 6) [18].

Problems of relatively low selectivity and redeposition of sputtered material can be eliminated by adding a chemically reactive component to the mechanical sputtering process. If the material to be removed can be com-

combined with a component of the plasma or ion beam to form a high-vapor-pressure compound, it will be selectively removed without redeposition. The two most important reactions for this process are oxidization of carbonaceous material (i.e., polymers) and the formation of volatile halogen-containing compounds. A wide range of semiconductors including Si, GaAs, InP, and Ge as well as metals such as W, Mo, Cr, and Al can be etched in chlorine- or fluorine-containing plasmas.

Many of these plasma processes depend on ions as either reactants or as initiators of the surface reactions [80]. By directing these ions along electric field lines, the highly anisotropic etching necessary for good resolution is produced. Three closely related techniques, plasma etching, reactive-ion etching, and reactive-ion-beam etching, have been developed to incorporate these plasma processes. Oxygen has been used to etch organics, and CF_4 has been used for materials like Si, SiO_2 , and transition metals. Other halogen-containing gases, such as CCl_4 or Cl_2 , have been used where a different chemistry is needed.

Reactive-ion-beam etching is a conceptually simple process in which a sample in a vacuum is bombarded with a particle beam containing reactive species. Important parameters like beam energy, composition, and density can be independently adjusted, leading to a well-controlled and well-characterized process. Thus, reactive ion beams have been a valuable tool for studying the chemistry of plasma etching processes [81].

Though reactive-ion-beam etching is conceptually simple, it is difficult to implement over large areas. The related processes of plasma etching and reactive-ion (sputter) etching have proved more versatile and are easier to scale to large areas. In reactive-ion etching, the sample is placed on the powered electrode of a conventional rf diode sputtering system containing a reactive plasma. Pressures usually range from about 1 to 100 mTorr, with power densities of about 1 W/cm^2 at 13.56 MHz. Positive ions in the plasma are accelerated across the cathode fall region, striking the sample at normal incidence. Though mechanisms for reactive-ion etching and reactive-ion-beam etching are roughly similar, there is strong evidence that other processes can be important in addition to bombardment by active species. In particular, adsorbed species on the surface can be activated by bombardment from the plasma, leading to complex surface reactions [80]. Thus, specific results, such as etch rates, can be quite different for the two processes.

Both reactive-ion etching and reactive-ion-beam etching are generally very directional because of the directionality of the ions, but the mechanical sputtering component of the etch reduces the selectivity below that possible for many wet etches. Upper limits can be placed on the resolution of both processes by the successful fabrication of structures with dimensions below 40 nm [26, 72]. Figure 9 shows high-aspect-ratio struc-

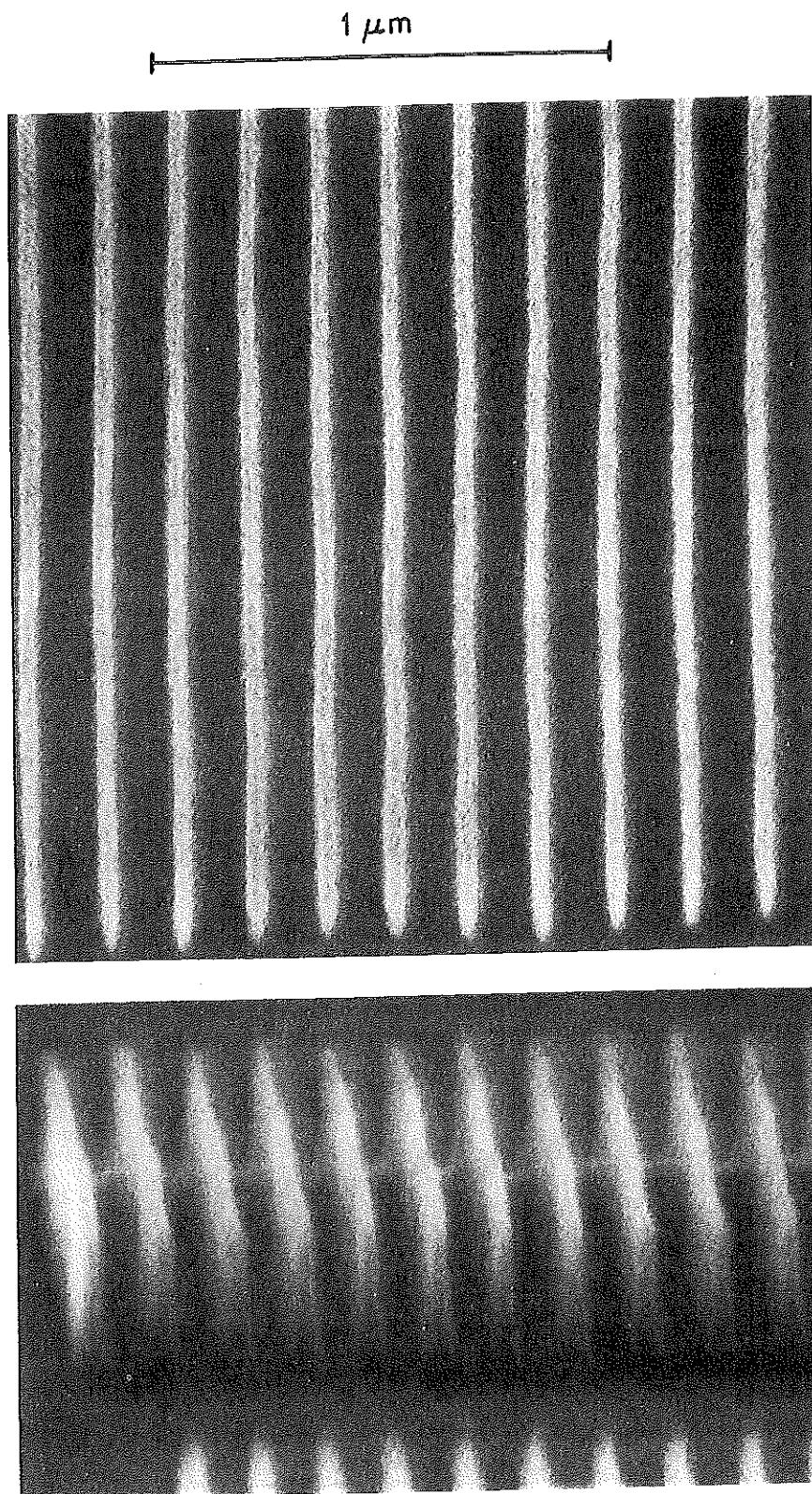


Fig. 9. Silicon structures formed by reactive-ion etching with CF_3Br . The Ni-Cr etch mask was patterned by lift-off with a trilevel resist stencil. (From work of Howard *et al.* [26].)

tures in Si formed by CF_3Br reactive-ion etching using a Ni-Cr etch mask. This mask was made by lift-off of an electron-beam-written trilevel stencil, as shown in Fig. 3. The fins of the etched Si structure are about 30 nm wide at the top, 300 nm deep, and spaced at a repeat distance of 140 nm. They are about 3 μm long (the dimension into the plane of the figure). Since the linewidth is determined by the original mask, the resolution limits of the etching process have not yet been reached, though it is clear that at this size scale the etching is not perfectly vertical.

Plasma etching is similar to reactive-ion etching, except that higher pressures and much lower ion energies are used. As a result, the etch has a lower sputtering component. At the pressures used (0.1 to > 1 Torr), there can be a significant isotropic component to the etch from neutral species in the plasma. With some materials, though, etching by ions or ion-assisted processes dominates, and anisotropy is possible. Under the proper conditions, the low energy of the ions and atoms in the plasma can make this a much more chemically selective process than reactive-ion etching, though not as generally useful for ultrahigh-resolution patterns.

IV. THREE-DIMENSIONAL TECHNIQUES

A variety of planar lithographies have been described that can either generate or reproduce features smaller than 100 nm, but these do not represent the only, or even the first, processes with this resolution. In the following sections a variety of techniques will be presented that take advantage of nonplanar processing to extend lithographic resolution and fabricate the kind of complete, multilevel structures necessary for many types of devices.

A. Edge-Defined Structures

The fabrication process with the highest resolution is the growth or deposition of a thin film, where dimensions can be controlled to better than 1 nm. Examples of very thin films are common even in current technology. For example, SiO_2 film thicknesses below 100 nm are easily made, as are metal films or diffusion profiles. Though these might seem trivial examples of microfabrication, processes have been developed for "folding over" this vertical dimension onto a lateral dimension on the substrate where the extremely high resolution can be used in complex devices. The power of such techniques is clearly apparent when optical lithography can be used to make devices with minimum feature sizes of 30 nm [82].

Though both electron-beam and x-ray lithography can produce metal lines less than 50 nm wide for scientific studies, the smallest such microwires to be studied electrically have been made using optical lithography combined with various tricks of three-dimensional processing to fabricate the wires [82, 83]. These represent some of the simplest (and the most elegant) three-dimensional processes and will serve as a general introduction to the concepts.

1. Wires and FET Gates

The most direct way of transforming a vertical dimension into a lithographic dimension is to use a simple step edge and either fabricate a device on the edge or use some directional process to shadow this edge onto the horizontal surface. Figure 10 shows a side view of such a step, produced with ion-beam or reactive-ion etching, and illustrates the various shadowing processes possible. If a film is deposited from behind the edge using evaporation from a "point" source, the shadow of the edge leaves a gap in the film whose width is determined by the step height and the angle of evaporation. This gap can then be incorporated in a device structure as, for example, an electrode gap in a CCD circuit [84]. Alternatively, the evaporated film can be used as a stencil mask for a subsequent evaporation of a second material. Single wires [85] and submicrometer dual-gate FETs [86] have been made using this technique. Though neither of these examples includes linewidths below 100 nm, they do not necessarily

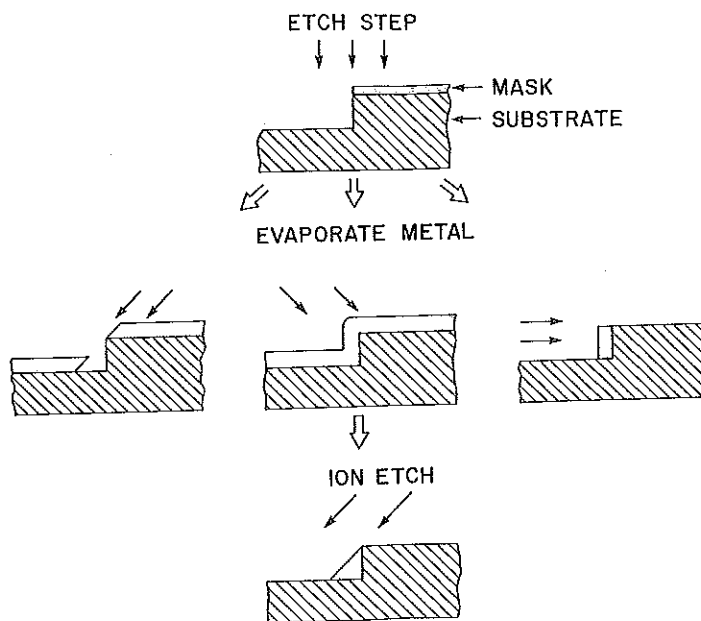


Fig. 10. Wire or gap formation on a step. (See text for discussion.)

achieve the limiting resolution of the process. A good review of three-dimensional fabrication techniques used for micrometer-sized structures is by Nathanson and Goldberg [87].

In the process just described, lift-off was used to reverse the tone of the shadow; etching can also perform the same function, as shown in the center of Fig. 10. In this case, the edge of the step is uniformly coated, and the step is then used to protect the material in its shadow from ion etching. In the process developed by Prober *et al.* [82], steps were formed by CF_4 or Ar ion-beam etching of a glass substrate, using a chrome etch mask patterned by photoresist lift-off [44]. Since the resist stencil was made using optical lithography, the etched step was somewhat irregular on the scale of 10 to 15 nm, though the edge profile of the step was square to much better than that. In spite of small edge irregularities, the self-aligning properties of this technique generate a wire with a uniform cross section. Wires as small as 25 nm across and 300 μm long have been made for fundamental studies of electron localization [88, 89].

The complementary process to using the shadow of a step is the fabrication of a structure directly on the edge of the step [30, 82, 83]. Wires of this kind have been made by evaporating a metal film parallel to the surface, as shown in Fig. 10. Wires with dimensions as small as 30 nm \times 30 nm have been produced for studies of electron localization [83]. A transmission electron micrograph of such a wire on a membrane substrate is shown in Fig. 11. Clearly, the edge roughness is sufficiently small to allow fabrication of wires as small as 10 nm if continuous, fine-grained metal films are used.

Using techniques like those in Fig. 10, one can also fabricate very short FET gates for use in studies of device scaling. Such a process was developed by Jackson and Masnari [90]. The deposition was done using selective electroplating on the edge of a conducting film, producing a fine wire for use as a Schottky gate in a GaAs MESFET. Polysilicon etch masks have been used to pattern gate electrodes as narrow as 100 nm for Si MOSFETs [91] using a process similar to that shown at the bottom of Fig. 10 to form the etch masks. The gate is used also as a mask for a self-aligned ion implantation of the source and drain regions. Similarly, Al lines as narrow as 60 nm with aspect ratios greater than 5 to 1 have been fabricated by evaporation on the edge of a photoresist pattern with an undercut profile, followed by lift-off of the unwanted metal by dissolving the resist [92]. With this process, ion etching and the attendant degradation of MOSFET properties is avoided. Finally, x-ray masks with linewidths below 10 nm have been made by edge evaporation, as described in Section III.D and shown in Fig. 8.

In the preceding examples of FET fabrication, the conducting channels

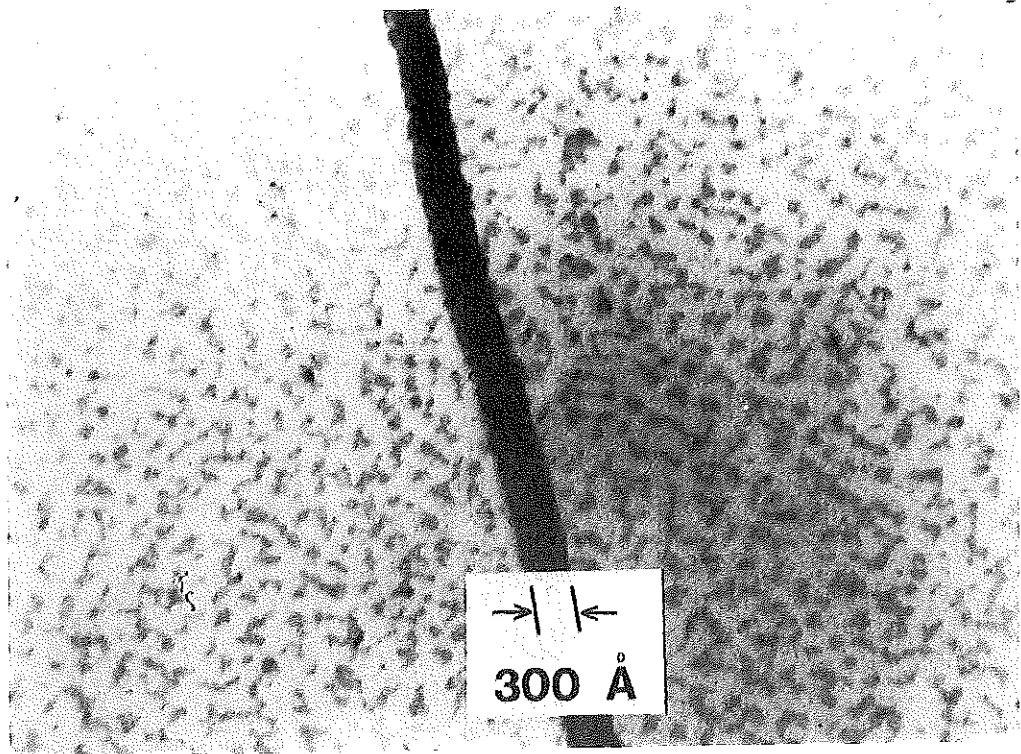


Fig. 11. Rectangular Ni wire, with 30-nm linewidth, formed on the edge of a step in SiO_2 . (From Flanders and White [83].)

were short (along the direction of current flow) but not narrow. Devices in which both lateral dimensions are small are required for high-density circuits. The smallest of these to date has been fabricated with electron-beam lithography [93].

2. Microbridges

The “three-dimensional” techniques described so far have involved constraining the device size in essentially only one dimension. These processes are, in fact, rather straightforward examples of shadowing methods. It is also possible, using two steps in the substrate, to produce more complex structures that are small in two lateral dimensions. The main example of this is work by Feuer and Prober, who fabricated a complete superconducting microbridge device, including leads and active region, using just shadowing of steps [72, 73, 94]. In this work, the “jog” at the intersection of the two etched steps (see Fig. 12) formed the pattern over which the microbridge was deposited. The jog, therefore, determined subsequent microbridge dimensions. The steps were formed sequentially in the substrate using CF_4 reactive-ion-beam etching, with pho-

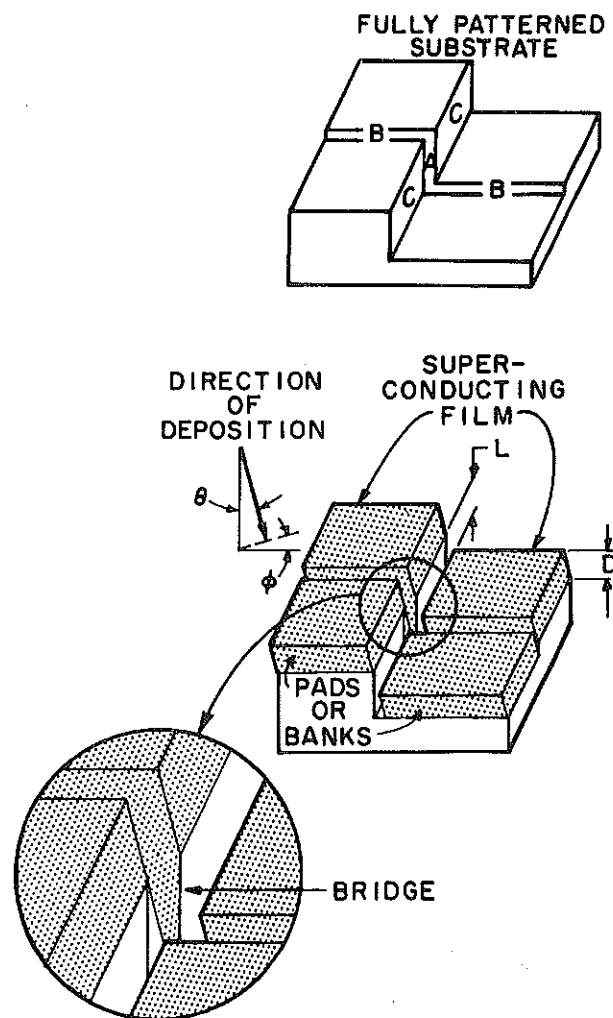


Fig. 12. Edge-defined superconducting microbridge. Formation of the fully patterned substrate is described in Feuer and Prober [72]. Bridge thickness is not shown. (From Feuer and Prober [72].)

tolithographic lift-off patterning [44] used to define the etch masks. The patterned substrate that results is shown in Fig. 12. Evaporation of a superconducting Pb-In film at the appropriate angle forms thick contact pads at the upper and lower surfaces while connecting them with a thinner bridge, the device of interest, along the face of the jog (region A). The thick contact pads significantly improved the cooling of the bridge, as compared with a device structure with thin contact pads. Such improved microbridges may be used as very high frequency detectors [94].

With the approach shown in Fig. 12, three-dimensional bridges as small as 50 nm in all dimensions have been made [73, 94]. Other step-edge fabrication approaches for producing superconducting microbridges have

also been developed. These techniques have recently been reviewed [95]. The essential idea in all these approaches is to achieve high resolution by using a pattern etched into the substrate, rather than developed in a resist, to define the structure. This also allows heated-substrate deposition, as is required for the superconducting films of greatest technical interest [95, 96].

3. Tunnel Junctions

In addition to simply defining conductor dimensions, step edges have been used to make a number of small-area tunneling structures. Both Havemann [97] and Heiblum *et al.* [98] have studied metal–oxide–metal (MOM) structures having nonlinear current–voltage characteristics with application to high-frequency mixing and detection. Similar structures using superconducting electrodes have also been investigated both as high-frequency mixers and detectors (~ 100 GHz) and for application to digital logic circuits [99–101]. In these applications, an important consideration is to reduce the device RC time and thereby improve frequency response. This can be accomplished by reducing the area, and thus the capacitance C of the tunnel junction. The resistance R is kept constant, and because the conductance of a tunnel barrier increases exponentially with decreasing barrier thickness, large reductions in area can be compensated by small changes in the oxide thickness. The RC time therefore decreases nearly in proportion to the area reduction.

Figure 13 shows the basic structure used to make a small-area, edge-defined tunnel junction. A step edge consisting of a thin metal film covered by a relatively thick insulator is formed by successive deposition of the layers and patterning with either lift-off or etching. After the edge of the metal film is exposed, the tunneling oxide is formed and a counter electrode is deposited. The active area of the device is limited to the edge of the base electrode, and the junction area is determined by the thickness of

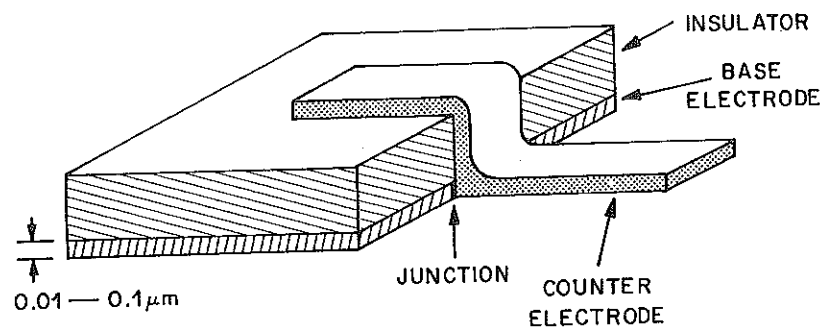


Fig. 13. Edge-defined tunnel junction. (From Howard [12].)

the base electrode and the width of the counter electrode as defined by conventional lithography. Using optical lithography and a 10-nm-thick Ni base electrode, MOM devices as small as 10^{-10} cm² have been made [98]. Also with optical lithography, edge-defined Pb-alloy superconducting devices as small as 10^{-9} cm² have been made [101]. With electron-beam lithography, Nb-based superconducting devices as small as 3×10^{-10} cm² have been made [102].

The edge-defined processes discussed in this section are all examples of a larger class of techniques that depend on directional deposition or etching. Though such processes were developed to reduce linewidths below that available in a given lithography, they also offer a number of other advantages. Because the processes are self-aligning, they are, in general, very reproducible and have a high yield of good devices. The improved resolution is also usually obtainable over a much larger area than the area over which the direct lithography (i.e., optical or electron beam) has the highest resolution. This improvement results from the enhanced edge definition of high-contrast processes such as lift-off and ion etching. With such edge definition, the three-dimensional techniques can be employed to full advantage. With the resolution that is achieved, some tens of nanometers, device dimensions are often limited only by film properties.

B. Self-Aligned Device Fabrication

The edge-defined processes discussed in Section IV.A are most appropriate for simple structures in which one dimension must be very small. Other techniques have been developed to fabricate complete, fully self-aligned devices. These processes include aspects of the edge-defined approaches, often in conjunction with multilevel resist techniques.

A general remedy to the limits on alignment capability of any exposure method is to use a single lithographic step to define multiple layers of a device [103]. A familiar example of this is to use the gate of a MOSFET as the mask for ion implantation of the source and drain. This ensures perfect alignment even in the presence of large-scale wafer distortions. Silicon MOSFETs as small as 100 nm have been made this way [91].

Superconducting tunneling devices provide a second example of such self-aligning processes. They are particularly suitable for fabrication with polymer stencils because complete devices can be made using film deposition and oxidization processes carried out at temperatures near ambient.

For fabricating small tunneling devices, Dolan [104] developed a lift-off process based on the three-level resist stencil used by Dunkleberger [47]. Because the lower layer of the stencil can be undercut without signifi-

cantly changing the pattern in the upper layer, it is possible to remove completely the lower layer of resist from underneath a "bridge" in the upper resist layer. With a properly designed pattern, these bridges will have sufficient support at either end to ensure rigidity.

Figure 14 shows a schematic of such a suspended resist mask as used to make a superconducting tunnel junction. The base electrode of the tunnel junction is first evaporated from angle 1, followed by oxidization of that film. The second electrode is then deposited from angle 2, chosen to give a small overlap between the two films. With careful control of the angles and the resist thickness, overlap structures with areas as small as 10^{-9} cm^2 can be made using optical lithography [105]. Such devices have been extensively studied for use as millimeter-wave detectors [105–107].

Even better control of the area of the device can be obtained [101] by using the edge-defined technique shown in Fig. 13 in combination with evaporation through a resist stencil. For example, the insulator in Fig. 13 can also be evaporated through the suspended stencil before the deposition of the counter electrode. With the proper choice of angles, only the edge of the base electrode will be exposed and, thus, the degree of lateral overlap of the two metal films is not critical. With this technique, superconducting Pb-alloy junctions as small as 10^{-9} cm^2 have been made routinely, using only optical lithography [101, 108].

If a high-resolution *electron* resist bilayer is used for the process in

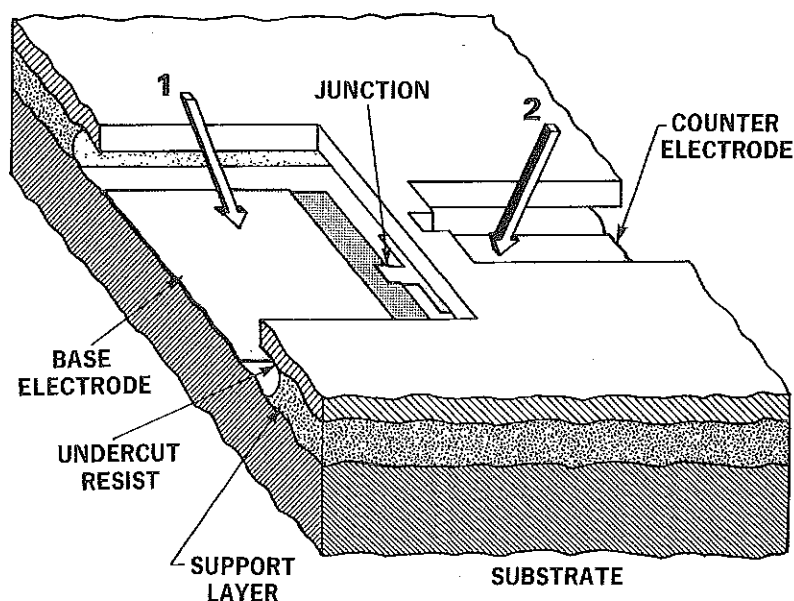


Fig. 14. Self-aligned tunnel-junction fabrication, patterned with a multilayer resist stencil. The base electrode is oxidized prior to deposition of the counter electrode. (Following Dolan [104].)

Fig. 14, tunnel junctions can be formed at a much smaller scale than can be accomplished with optical resists. Figure 15 shows a Josephson tunnel junction with a Pb–In base electrode and a Pb counter electrode made using such an electron resist process [42, 109]. The complete device is less than 100 nm on a side and has an area of 10^{-10} cm². It has sufficiently low capacitance to exhibit essentially nonhysteretic I – V characteristics, unlike the hysteretic latching behavior observed in larger junctions. The

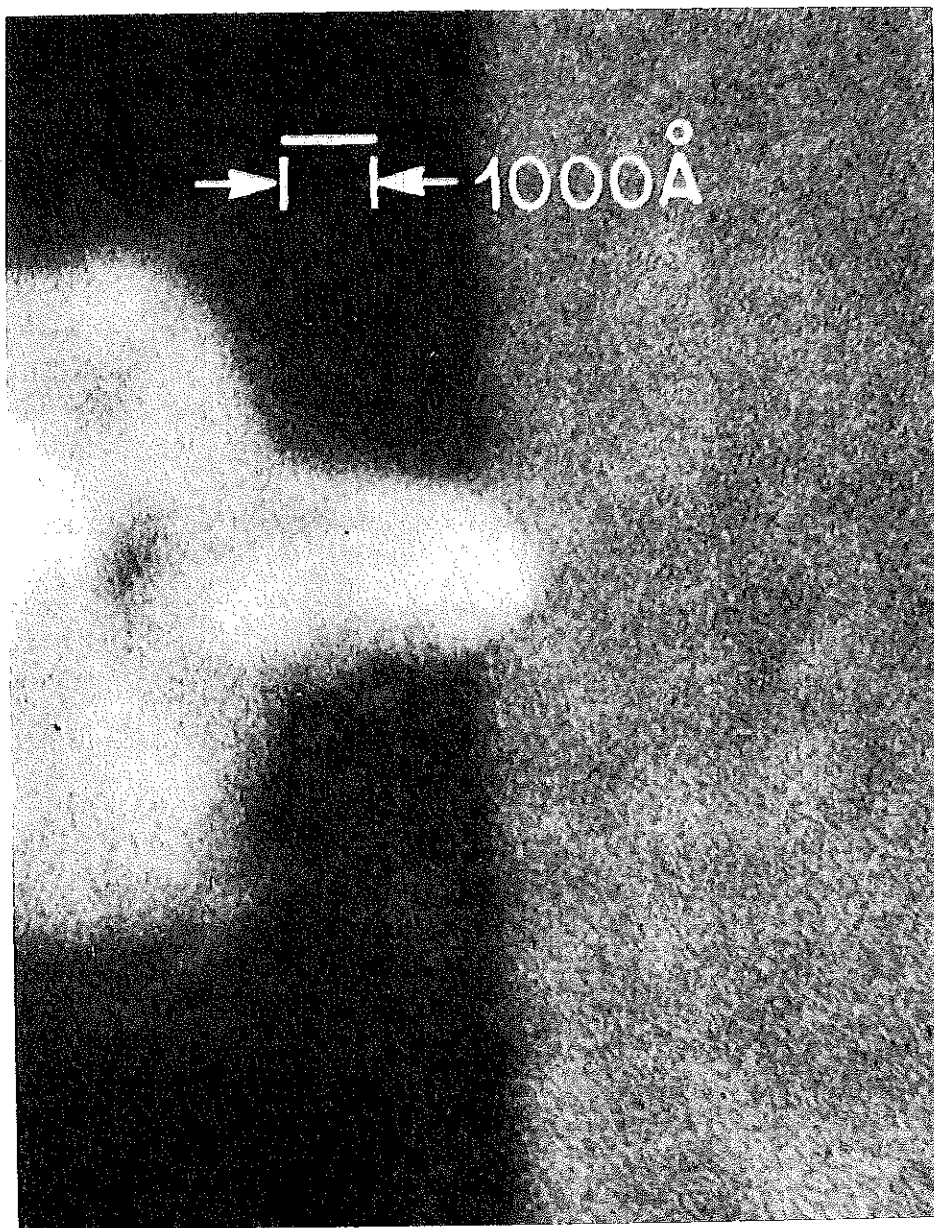


Fig. 15. Small tunnel junction made by oblique evaporation through an electron-beam patterned stencil, as in Fig. 14. (From Hu *et al.* [42].)

TABLE VIII

Final Pattern Resolution Achieved with Three-Dimensional Techniques

Technique ^a	Process	Resolution achieved (nm)	Refs. ^b
Edge defined	Triangular wire, ion etched	30	a
	Rectangular wire, deposited	30 × 30	b
	MOSFET gate	100	c
Self-aligned structure	Tunnel junction	~100 × 100	d

^a All structures were produced on a thick substrate.^b References:

- a. Prober *et al.* [82]
- b. Flanders and White [83]
- c. Hunter *et al.* [91]
- d. Hu *et al.* [42]

device in Fig. 15 is, to our knowledge, the smallest multilayer electronic device produced to date by any method. This junction, and the other high-resolution structures made with three-dimensional techniques, are listed in summary in Table VIII.

C. Fabrication Limits

The three-dimensional techniques discussed in this section would all seem to permit fabrication of structures smaller than 10 nm. However, there are a variety of effects that limit their resolution. The most obvious is penumbra due to limited collimation of the ion beam or evaporant flux. This effect can be eliminated, at the cost of reduced flux, by simply using apertures or moving the source further from the sample. (Diffraction effects are negligible.) Film residue or scattered atoms from the deposited films can cause serious problems, however, because high-contrast etching processes are typically employed. In our experience, this is a common problem, and one that is often hard to diagnose at these size scales. Careful shielding and cleaning of the deposition apparatus is essential.

A more fundamental limit for ion-beam etching occurs because sputtered atoms are ejected from a finite volume of the substrate. This region has been estimated to be as large as 10 nm in diameter [110], but careful measurements have not yet been made. These limits are also not yet well defined for processes using chemically active species such as reactive-ion etching or reactive-ion-beam etching. Very low energy etching processes [81] may offer some improvement. Additional limitations are imposed by

the microstructure of the material being etched. Since sputtering rates can be expected to depend on local composition and crystal orientation, only single-crystal or amorphous substrates can be expected to show uniform erosion. However, it is also found that some polycrystalline materials can be polished, or smoothed, by ion-beam etching.

Deposition processes such as evaporation suffer from grain growth and surface migration problems. Adsorbed atoms tend to migrate across the surface before condensing into crystallites [111, 112], thus placing a resolution limit on any shadowing process. Because of this migration, there are relatively few materials that can be deposited with grain sizes below 10 nm on room-temperature substrates. Examples of fine-grained thin films are Au-Pd [89], Ni-Cr [26], W [30], and W-Re [113]. In a related phenomenon, some materials have been observed to form shelves out from the top of step edges and, thus, strongly modify the shadow on the lower surface. This has been seen even in some materials with relatively high melting points, such as Cr [73] and Mo [114].

Finally, any thin-film structure must be stable against interdiffusion or reaction with adjacent layers. For dimensions smaller than 10 nm, this places strong limits on the materials and processing temperatures. For example, holes smaller than 10 nm formed in NaCl microcrystals by direct electron-beam etching are found to refill spontaneously at room temperature, presumably by surface migration [11]. At such size scales, surface energies, thermal motion [112], and diffusion phenomena that are unimportant for micrometer-sized structures can predominate.

V. CONCLUSIONS

We have seen in this chapter that the tools now exist to fabricate general structures much smaller than 100 nm. Direct beam writing with electrons and ions, printing with x rays, and edge-defined techniques can all produce metal structures as small as ~ 20 nm; 10-nm dimensions are possible, with care, for specific materials. Work still remains to be done on the damage effects [115] that can result with such high-energy patterning techniques.

Although patterning at dimensions < 100 nm is now feasible, at these dimensions semiconductor devices can be expected to behave in a non-classical manner or even fail to work at all. Also, it is difficult to control lateral doping profiles with the < 100 -nm resolution with which metal lines can now be patterned. Superconducting devices can be patterned at a size scale < 100 nm, and their performance continues to improve as device size is reduced below 100 nm. Superconducting devices have therefore

formed an ideal proving ground for testing advanced lithography approaches and have motivated development of many of these approaches.

The new lithography techniques described in this chapter can be used to produce new types of devices [1] and to study new physical phenomena that depend critically on the small size. An example of such a new physical phenomenon is the localization of electron wave functions seen in "one-dimensional" wires [88, 89, 113]. For wires with diameters less than 10 nm, such effects could be predominant at very low temperatures. Although such localization effects may themselves never limit computer performance (a wire resistance greater than 10 k Ω is required), localization effects may have device possibilities that can be exploited.

A major theme of this chapter is the utilization of the third dimension and new three-dimensional lithographic approaches. Such approaches are of clear advantage for achieving high-aspect-ratio patterns, high resolution, and good linewidth control over a large field of view. When three-dimensional approaches are combined with other self-aligning or self-limiting processes, very powerful device microfabrication approaches can be developed [103].

At present, advanced electron-beam lithography on thick substrates [26] approaches the resolution of recent edge-defined methods. These electron-beam techniques include, however, many features of the three-dimensional approaches. Anisotropic reactive-ion etching and multilevel resists are employed. Thus, advances in "planar" patterning capabilities and three-dimensional approaches are now intimately and successfully linked.

For the near future, general structures of ~ 20 nm size represent the approximate lower limit for current techniques. Thus, even though we can see structures smaller than 1 nm and can even visualize atomic motion [116], it does not appear possible to fabricate general structures at a 1-nm size scale by an extension of current techniques. Still, it seems reasonable that, in the future, atomic-scale building techniques, possibly a derivative of those used in molecular-beam epitaxy [117, 118], could allow fabrication of general structures with lateral dimensions < 10 nm in size. Though such atomic-scale building techniques remain to be conceived and demonstrated (in other than biological systems), the phenomenal progress of the last thirty years allows little room for pessimism.

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