

# Electronic analogs of double-junction and single-junction SQUIDs

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We describe electronic analogs of a double-junction (dc) SQUID and a single-junction (rf) SQUID that are simple to construct and operate, and are considerably more flexible than those previously reported. The Josephson junction analog is based on the Resistively-Shunted Junction (RSJ) model, and uses a novel method based on a sample-and-hold circuit to generate the  $\sin \theta$  "supercurrent." Examples are shown of the single-junction I-V characteristics, threshold curves of critical current vs applied flux and I-V curves for the double-junction SQUID analog, and rf SQUID characteristics as a function of applied flux and rf drive current. Other applications of the analogs, including the incorporation of a nonsinusoidal current-phase relation, are discussed.

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## INTRODUCTION

Superconducting quantum interference devices (SQUIDs) have in recent years been employed in a wide variety of sensitive electromagnetic devices, and have demonstrated on a macroscopic scale a number of basic quantum effects. SQUIDs have been used to construct extremely sensitive voltmeters and magnetometers,<sup>1</sup> and are under active development as switching and memory devices for a new and faster generation of digital computers.<sup>2</sup> A detailed understanding of the behavior of SQUIDs and the Josephson junction devices on which they are based is therefore of considerable importance. Because the Josephson junction devices employed in these circuits are described by nonlinear differential equations, the development of an understanding of the circuit behavior has to a large extent been accomplished either by extensive calculations<sup>3</sup> on digital computers or by working with mechanical<sup>4</sup> or electronic<sup>5-7</sup> analogs.

While digital computers are of undeniable value in obtaining specific numerical results, the time spent in writing, debugging, and running computer programs to solve the properly-scaled coupled differential equations is not insignificant. Electronic analogs have an advantage in demonstrating qualitative behavior quickly over a wide range of parameters and can usually give quantitative results to a precision of a few percent. Furthermore, the electronic analogs we describe here can be breadboarded from readily available parts and made to work in a day or two by someone with a working knowledge of integrated circuits. As compared with mechanical analogs, in electronic analogs changes in junction and circuit parameters can be made easily and interaction of the junction with time-dependent applied currents or voltages can readily be studied.

We present here an electronic Josephson junction analog of the phase-locked-loop type introduced by Bak and Pederson,<sup>5</sup> but with an improved method of obtaining a current proportional to  $\sin \theta$  and an improved method of summing the supercurrent, quasiparticle current, and displacement current. We also show how to obtain a voltage proportional to the quantum-phase difference  $\theta$ , and how to use this voltage in constructing analogs of double-junction and single-junction (rf) SQUIDs based on the resistively-shunted-junction model<sup>3</sup> for the individual junctions. Nonzero loop inductance is included in these analogs. Finally we exhibit some representative characteristic curves for each type of SQUID. Another application of the junction analog, which incorporates a nonlinear quasiparticle current to simulate the behavior of an oxide-barrier Josephson tunnel junction, will be discussed in a separate article.<sup>8</sup>

While there has been a relatively large number of electronic analogs of single Josephson junctions described in the literature,<sup>5</sup> we know of only one previous article that has described an rf (single-junction) SQUID analog<sup>6</sup> and only one that has described a double-junction SQUID analog.<sup>7</sup> Both of these circuits are considerably more complex than ours. For example, Tuckerman's analog of a double-junction SQUID uses multiple floating power supplies in simulating inductances and requires a number of very critical adjustments. We believe that because of their relative simplicity, the analogs described in this paper will be of use both as instructional tools and in exploratory circuit design.

For certain applications, one may require a single-junction analog in which the junction current is injected at the same point as that where the junction voltage is measured. The junction analog we develop in the main body of this work would not be appropriate in such applica-

tions. An appropriate junction analog is presented in Appendix B. That analog utilizes the improved method for obtaining the  $\sin \theta$  supercurrent, but uses the current summing method of Bak and Pederson.<sup>5</sup>

## I. THE JOSEPHSON EQUATIONS

The supercurrent flow  $I_s$  through a Josephson junction is described by the two Josephson equations<sup>9</sup>

$$I_s(t) = I_c \sin \theta(t), \quad (1)$$

and

$$d\theta/dt = 2\pi V(t)/\phi_0, \quad (2)$$

where  $\theta$  is the quantum phase difference between the superconducting order parameters (pair wavefunctions) on the two sides of the junction,  $I_c$  is the geometry-, temperature-, and material-dependent maximum supercurrent,  $\phi_0$  is the flux quantum  $h/2e = 2.07 \times 10^{-15}$  V s, and  $V(t)$  is the time-dependent voltage across the junction.

In addition to this supercurrent of Cooper pairs, for nonzero voltages there is a current of quasiparticles ( $\approx$  single electrons) which is often modeled by the current through an ordinary ohmic resistor  $R$ . The resulting *resistively-shunted-junction* (RSJ) model of a Josephson junction was introduced by Stewart and McCumber<sup>3</sup> and is widely used in both analytical and computer studies of Josephson junctions and SQUIDS. While junctions of the microbridge or point contact type are characterized fairly well by the RSJ model, tunnel junctions are not, because the quasiparticle current-voltage characteristic is highly nonlinear. Although it is possible to incorporate models of the nonlinear quasiparticle conductance of a tunnel junction into our circuits,<sup>8</sup> we confine the present discussion to the RSJ model.

If we include the stray capacitance  $C$  across the junction, the total junction current  $I$  is given by

$$I = I_c \sin \theta + V(t)/R + C dV/dt, \quad (3)$$

which, along with Eq. (2), gives a complete characterization of the resistively shunted junction.

## II. ELECTRONIC ANALOGS

### A. Single Josephson junction

Figure 1 shows the electronic analog developed for a single junction. The operational amplifier in Fig. 1(a) is in the standard inverting configuration. The virtual ground approximation<sup>10</sup> applies; the negative terminal is at ground potential and the sum of the currents into the negative terminal is zero. Therefore the bias current  $I$  is related to the currents in the three feedback paths by

$$I = (\sin \theta)/r' + V/R + C dV/dt. \quad (4)$$

The electronic circuit is thus an exact analog of the Josephson junction described by Eqs. (1) and (2), provided we can generate a voltage equal to  $\sin \theta$ . Comparing Eqs. (3) and (4), we see that the op-amp output voltage, measured with respect to ground, is the analog of the junction voltage, and  $1/r'$  corresponds to the critical current  $I_c$ .

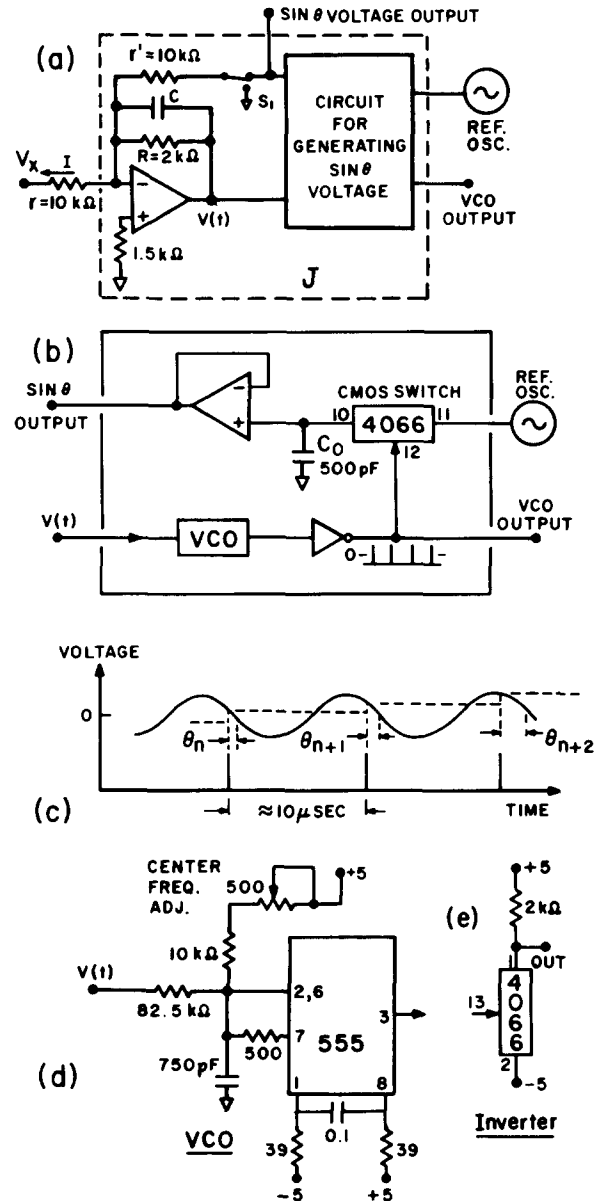


FIG. 1. (a) Circuit analog for a resistively-shunted Josephson junction, Eqs. (4) and (5). The grounded position of switch  $S_1$  is used when matching the VCO and reference oscillator frequencies. Junction current  $I = -V_x/r$ . (b) Circuit for generating a voltage equal to  $\sin \theta$ . When the control voltage  $V(t)$  of the VCO is zero, the reference oscillator is sampled once each cycle of its sinusoidal output and  $\sin \theta$  is constant. The 555 timer and CMOS 4066 are powered by the  $\pm 5$  volt supply (i.e., not by 0 and +5 volts). The output voltages of the timer and the inverter (pin 1 of 4066) therefore switch between approximately +5 and -5 volts. (c) Showing the effect of a slightly positive  $V(t)$ . The sinusoid is sampled slightly earlier each cycle, producing a staircase wave which rises and then falls, closely approximating  $\sin \theta(t)$ . (d) Details of the VCO circuit of (b). The center frequency of the 555 timer is adjustable. The timing is determined by the alternate charging and discharging of the capacitor to the triggering thresholds,  $\pm 1.67$  volts. The 82.5 and 10 k $\Omega$  resistors are Corning type RN60D metal film (100 ppm/ $^{\circ}$ C variation). The 750 pF capacitor is silver mica. (e) Inverter circuit for use in circuit of Fig. 1(b). Op amps are type 741.

As in the electronic analog of Bak and Pederson, we model the quantum phase difference  $\theta$  by the phase difference between a voltage-controlled oscillator (VCO) and a fixed-frequency, sinusoidal reference

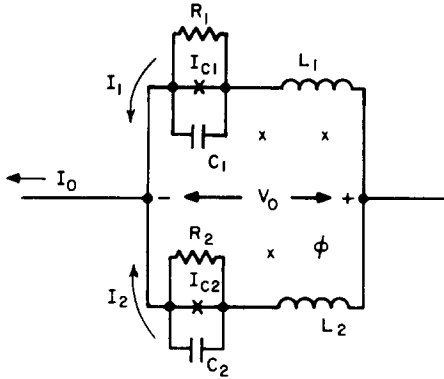


FIG. 2. Circuit model of a double-junction SQUID. —X— represents the supercurrent channel of a single RSJ model junction. The inductances are defined in terms of the flux  $\phi$  produced in the SQUID loop (perpendicular to the plane of the figure). Thus,  $\phi = L_2 I_2 - L_1 I_1$  plus any externally applied flux,  $\phi_{\text{ext}}$ . Our  $L_1$  and  $L_2$  correspond to  $\mathcal{L}_1$  and  $\mathcal{L}_2$  of Ref. 14, and include the effects of mutual inductance. Because the average voltage across  $L_1$  or  $L_2$  is zero, the average voltage  $\langle V_0 \rangle$  across the SQUID is equal to the average voltage across either junction.

oscillator of angular frequency  $\omega_0$ . If the VCO is adjusted to run at precisely the same frequency as the reference oscillator when its control voltage  $V$  is zero, and if the VCO frequency-voltage characteristic is linear, then for nonzero voltages the VCO angular frequency is given by  $d\theta_{\text{VCO}}/dt = \omega_0 + 2\pi V(t)/\lambda$ . The rate of change of phase difference between the VCO and reference oscillator is thus given by

$$d\theta/dt = 2\pi V(t)/\lambda. \quad (5)$$

Equation (5) is analogous to Eq. (2) with  $\phi_0$  replaced by  $\lambda$ .

Our method of generating  $\sin \theta$  is shown in Figs. 1(b) and (c). The idea is to sample the sinusoidal voltage from the reference oscillator once each cycle of the VCO wave and store this value on a capacitor  $C_0$ . Since the amplitude of the sine wave is adjusted to be 1 volt zero to peak, the set of sampled voltages closely approximates the continuous function  $\sin \theta(t)$ . With the reference oscillator and VCO running at about 100 kHz, the updating of the capacitor voltage occurs approximately every 10  $\mu\text{s}$ . Thus the sampled voltage at the output of the  $\sin \theta$  circuit is a staircase wave which lags the instantaneous value of  $\sin \theta$  by an average delay of  $\approx 5 \mu\text{s}$ , which is small compared with the time scale ( $\sim 1 \text{ ms}$ ) over which  $\sin \theta(t)$  and  $V(t)$  change.

This method of generating  $\sin \theta$  is an improvement over earlier methods that mix (multiply) the signals from the reference oscillator and the VCO and filter the mixer output with a low-pass filter (see Bak, Ref. 5). The filter introduces a phase shift (associated with the typical low-pass filter time constant of 100  $\mu\text{s}$ ) which is more than an order of magnitude larger than that associated with our sample-and-hold circuit. In addition, the mixer circuit is often a special purpose and relatively expensive integrated circuit whereas all the integrated circuits in our analog are inexpensive and readily available.

In Fig. 1(b) the VCO is a 555 timer configured as in Fig. 1(d). The sampling switch is one section of a CMOS 4066,<sup>11</sup> the inverter is made from another section of the

same switch [Fig. 1(e)], and the voltage follower is a 741 op amp, as is the main op amp of Fig. 1(a). Either a Hewlett-Packard 606A or a General Radio 1310-A was used as the reference oscillator. All of the integrated circuits are powered by a single  $\pm 5$  volt supply which consists of LM 7805 and LM 7905 integrated circuit regulators driven by a commercial  $\pm 15$  volt supply (see Fig. 13, below).

## B. Double-junction SQUID

Figure 2 shows a circuit model of a double-junction SQUID, in which the applied current  $I_0$  splits into currents  $I_1$  and  $I_2$  through the two junctions. The phase differences  $\theta_1$  and  $\theta_2$  across the two junctions are related to the total flux  $\phi$  through the SQUID loop by the well-known fluxoid quantization condition<sup>12</sup>

$$\phi/\phi_0 + (\theta_2 - \theta_1)/2\pi = 0. \quad (6)$$

Usually Eq. (6) is equated to an integer  $n$ . Without loss of generality we consider the specific case  $n = 0$  and allow  $(\theta_2 - \theta_1)/2\pi$  to exceed unity. Also, for simplicity we consider here the specific case of identical junctions, for which  $R_1 = R_2 = R$ ,  $C_1 = C_2 = C$ , and  $I_{c1} = I_{c2} = I_c$ . The total flux is the sum of an externally applied flux  $\phi_{\text{ext}}$  and the fluxes  $L_2 I_2$  and  $-L_1 I_1$  generated by the currents flowing in the SQUID loop. That is,

$$\phi = \phi_{\text{ext}} + L_2 I_2 - L_1 I_1. \quad (7)$$

In writing Eq. (7) we follow the notation of Fulton, Dunkleberger, and Dynes, Ref. 4. Our symbols  $L_1$  and  $L_2$  correspond to  $\mathcal{L}_1$  and  $\mathcal{L}_2$  of Tesche and Clarke, Ref. 14, and include the effects of both self-inductance and mutual inductance. Thus, the instantaneous induced voltages across  $L_1$  and  $L_2$  are *not* given by  $L_1 dI_1/dt$  and  $L_2 dI_2/dt$  but rather are linear combinations of  $dI_1/dt$  and  $dI_2/dt$ . However, we need not consider these voltages in our analysis because we are interested only in voltages averaged over the period of a Josephson oscillation. Such average voltages across  $L_1$  and  $L_2$  are zero.

Combining Eqs. (2), (3), (6), and (7) with Kirchhoff's current law, we arrive at the following six equations involving the variables  $I_1$ ,  $I_2$ ,  $\theta_1$ ,  $\theta_2$ ,  $V_1$ , and  $V_2$ :

$$I_1 = I_c \sin \theta_1 + V_1/R + C dV_1/dt, \quad [8(a)]$$

$$I_2 = I_c \sin \theta_2 + V_2/R + C dV_2/dt, \quad [8(b)]$$

$$d\theta_1/dt = 2\pi V_1/\phi_0, \quad [8(c)]$$

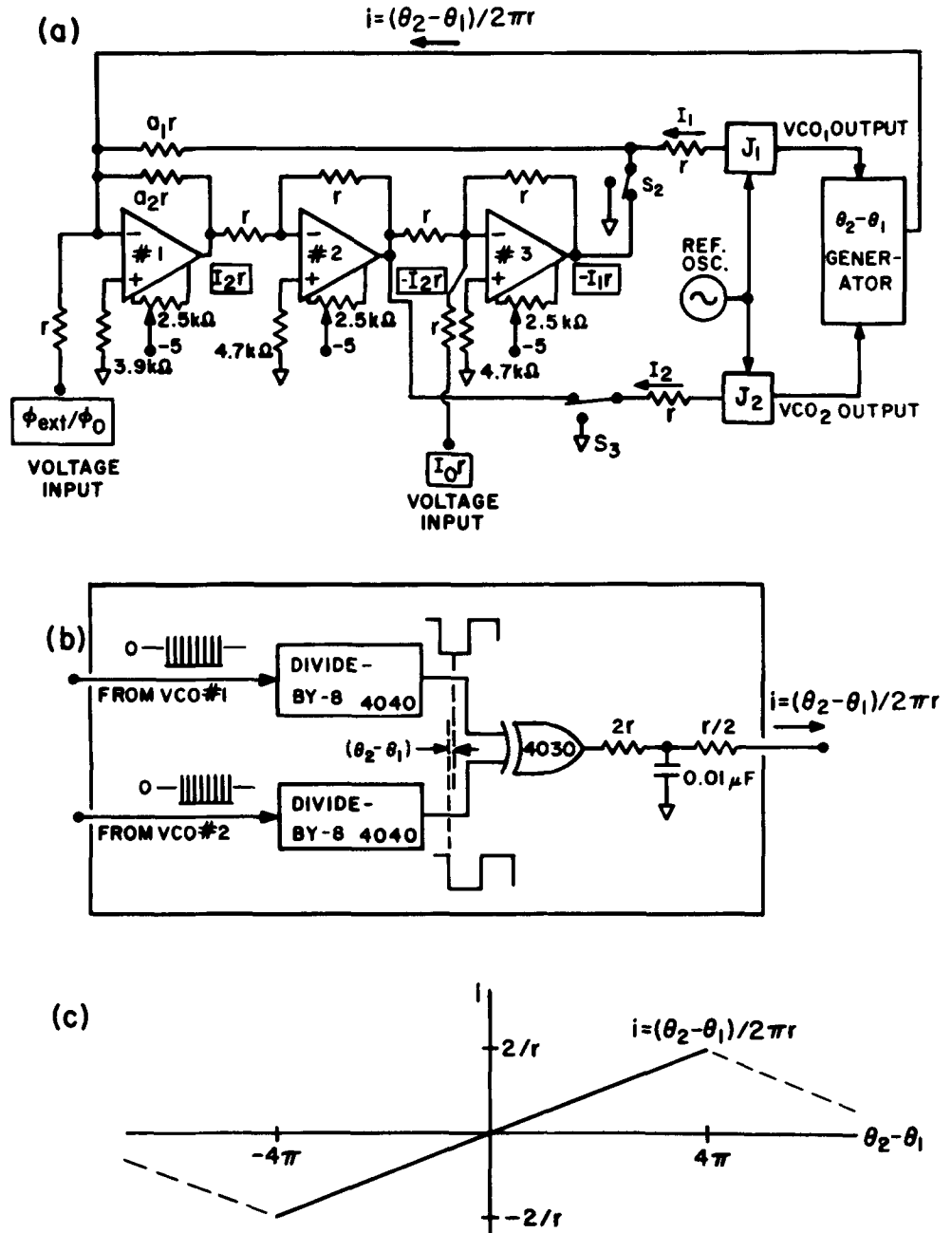
$$d\theta_2/dt = 2\pi V_2/\phi_0, \quad [8(d)]$$

$$I_0 = I_1 + I_2, \quad [8(e)]$$

$$\begin{aligned} \phi_{\text{ext}}/\phi_0 + (L_2 I_c/\phi_0) \times I_2/I_c \\ - (L_1 L_c/\phi_0) \times I_1/I_c + (\theta_2 - \theta_1)/2\pi = 0. \end{aligned} \quad [8(f)]$$

Figure 3(a) shows our analog of a double-junction SQUID. This contains a pair of junction analogs [Fig. 1(a)] that satisfy equations analogous to Eqs. [8(a)]–[8(d)]. The currents  $I_1$  and  $I_2$  in the analog are supplied by a circuit containing three op amps in a closed loop

FIG. 3. (a) Circuit analog of a double-junction SQUID. Each box labeled J contains the circuit within the dotted lines in Fig. 1(a) and is powered by its own  $\pm 5$  volt supply driven by a common  $\pm 15$  volt supply. All other circuits are powered by a third  $\pm 5$  volt supply. Currents are denoted by arrows; voltage values are enclosed in boxes.  $r = 10 \text{ k}\Omega$ . (b) The circuit for generating a current proportional to  $\theta_2 - \theta_1$ . The XOR output is a square wave of variable duty cycle. The resulting current is smoothed by the RC filter circuit. All integrated circuits are powered by a  $\pm 5$  volt supply. (c) The variation of current with phase angle for the circuit in (b). The circuit of Fig. 3(a) is a good analog of a double-junction SQUID provided  $|\theta_2 - \theta_1|$  does not exceed  $4\pi$ . See Appendix A for component selection.



configuration. These op amps constrain the currents to satisfy equations analogous to Eqs. [8(e)] and [8(f)]. Provided we can generate a current  $(\theta_2 - \theta_1)/2\pi r$ , the equations satisfied by the analog are

$$I_1 = \sin \theta_1/r' + V_1/R + CdV_1/dt, \quad [9(a)]$$

$$I_2 = \sin \theta_2/r' + V_2/R + CdV_2/dt, \quad [9(b)]$$

$$d\theta_1/dt = 2\pi V_1/\lambda, \quad [9(c)]$$

$$d\theta_2/dt = 2\pi V_2/\lambda, \quad [9(d)]$$

$$I_0 = I_1 + I_2, \quad [9(e)]$$

$$\phi_{\text{ext}}/\phi_0 + (r/a_2r') = I_2r'$$

$$- (r/a_1r') \times I_1r' + (\theta_2 - \theta_1)/2\pi = 0. \quad [9(f)]$$

Using the virtual ground approximation discussed previously, Eq. [9(e)] says that the currents into the invert-

ing input of op-amp #3 sum to zero. Op-amp #2 is a unity-gain inverter. Equation [9(f)] says that the currents into the inverting input of op-amp #1 sum to zero. In the second and third terms of Eq. [9(f)] we have multiplied and divided by  $r'$  [see Fig. 1(a)], which is numerically equal to  $r$ , in order to facilitate making identifications between quantities in Eqs. (8) and (9). These identifications are

$$\left. \begin{aligned} I_c &\rightarrow 1/r', \\ \phi_0 &\rightarrow \lambda, \\ L_2 I_c/\phi_0 &\rightarrow r/r'a_2 = 1/a_2, \\ L_1 I_c/\phi_0 &\rightarrow r/r'a_1 = 1/a_1, \\ I_1/I_c &\rightarrow I_1r', \\ I_2/I_c &\rightarrow I_2r'. \end{aligned} \right\} \quad (10)$$

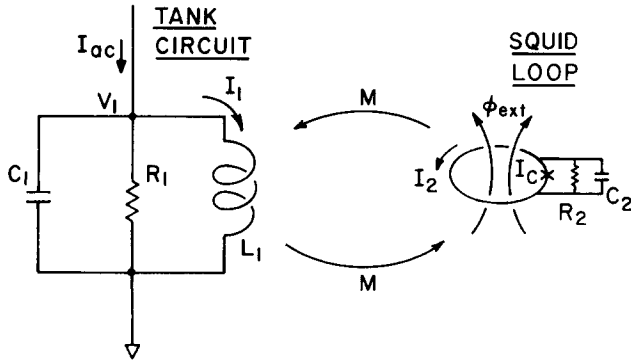


FIG. 4. Circuit diagram of a single-junction (rf) SQUID. The tank circuit and the SQUID loop are weakly coupled by the mutual inductance  $M$ . The average amplitude of the rf tank circuit voltage  $V_1$  is a function of both the tank circuit drive current  $I_{ac}$  and the externally applied flux,  $\phi_{ext}$ , linking the SQUID loop.

Thus, in the analog the voltages  $I_1 r'$  and  $I_2 r'$  represent the normalized currents  $I_1/I_c$  and  $I_2/I_c$  of the real SQUID.

The current  $(\theta_2 - \theta_1)/2\pi r$  is obtained from a phase-sensitive detector in which the output voltage is proportional to  $\theta_2 - \theta_1$  over the range  $-4\pi$  to  $4\pi$ . This phase-sensitive detector is illustrated in Fig. 3(b). It is simply an exclusive OR (XOR) logic circuit preceded by CMOS 4040 divide-by-eight counters, and followed by an RC low-pass filter. The inputs to this XOR circuit are square waves with logic 1 equal to 5 volts and logic 0 equal to  $-5$  volts. Although the output voltage of the XOR circuit switches rapidly between  $+5$  and  $-5$  volts, its average value varies linearly with the phase difference between its square wave inputs, from  $-5$  volts when these inputs are in phase to  $+5$  volts when they are  $180^\circ$  out of phase.

The divide-by-eight binary counters inserted between the VCO outputs and the XOR circuit serve three purposes. First, they convert the pulse outputs of the VCOs to symmetric square wave pulses necessary for operation of XOR phase detector. Second, they permit the VCO outputs to be in phase ( $\theta_2 - \theta_1 = 0$ ) when the outputs of the divide-by-8 counters are  $90^\circ$  out of phase. Third, and most important, they enable the voltage-phase characteristic of the detector to be proportional to  $\theta_2 - \theta_1$  over two complete cycles of phase difference in either direction from zero [see Fig. 3(c)]. If for some reason the magnitude of the phase difference becomes greater than  $4\pi$ , the averaged XOR output current begins to decrease linearly, the entire characteristic being a triangular wave with period  $16\pi$  [Fig. 3(c)]. Thus, the entire analog is limited to phase differences for which  $|\theta_2 - \theta_1| < 4\pi$ .

It is important to realize that an alternate method of obtaining a  $\theta_2 - \theta_1$  voltage, by integrating  $V_1$  and  $V_2$  to obtain voltages proportional to  $\theta_1$  and  $\theta_2$  and then subtracting these voltages, would be an unsatisfactory way of obtaining  $\theta_2 - \theta_1$ . This is because, even if  $\sin \theta_1$  and  $\sin \theta_2$  were individually to remain constant, meaning that both VCOs were locked to the reference oscillator frequency, drifts in the integrators would cause the  $\theta_2 - \theta_1$  voltage to change. Indeed, the integrator outputs representing  $\theta_1$  and  $\theta_2$  could eventually saturate. This problem

was recognized by Tuckerman,<sup>7</sup> who abandoned the phase-locked-loop approach and devised another method, which is considerably more difficult to build and adjust than is ours. In our analog, when  $\sin \theta_1$  and  $\sin \theta_2$  are constant, the fact that the phases of the VCO outputs are fixed relative to the reference wave assures that the phases are fixed relative to each other, and that the  $\theta_2 - \theta_1$  current remains constant.

### C. Radio-frequency SQUID

The circuit diagram of an rf SQUID, which is widely used to measure weak magnetic fields and is commercially available, is shown in Fig. 4. It consists of a radio-frequency current-driven tank circuit magnetically coupled to a superconducting loop containing a Josephson junction. When an rf current,  $I_{ac}$ , is first applied to the tank circuit the rf current  $I_1$  in the inductance begins to build up with a time constant of perhaps 20 periods of the rf frequency. As  $I_1$  increases, the rf flux in the SQUID loop produced by  $I_1$  induces an increasing rf current in the loop. At first this current flows through the Josephson junction almost entirely as supercurrent because  $d\theta/dt$ , and hence the junction voltage and the quasiparticle current, through  $R_2$ , are small. But when the peak supercurrent exceeds  $I_c$ , voltage pulses are developed across the junction which dissipate energy in  $R_2$ . This energy loss is reflected back into the tank circuit and results in a sudden decrease in  $I_1$ . The current  $I_1$  then starts to build up again and the cycle repeats. The net result is a time-average rf voltage amplitude across the tank circuit which saturates at a value  $V_1$  due to the energy loss in the junction. The amplitude of this saturated voltage is a function of both the amplitude of the rf driving current applied to the tank circuit and the external low-frequency or dc magnetic flux  $\phi_{ext}$  linking the SQUID loop. We return to a discussion of the dependence of  $V_1$  on  $\phi_{ext}$  and the tank circuit drive current in Sec. III.

The equations that govern the rf SQUID are written in terms of the following five variables: the tank circuit voltage  $V_1$ , the current in the tank inductance  $I_1$ , the voltage  $V_2$  across the Josephson junction, the SQUID loop current  $I_2$ , and the quantum phase difference  $\theta$  across the junction. The tank circuit drive current  $I_{ac}$  and the externally applied (low frequency) flux  $\phi_{ext}$  in the SQUID loop are regarded as independently adjustable parameters. The five rf SQUID equations are

$$I_{ac} = I_1 + V_1/R_1 + C_1 dV_1/dt, \quad [11(a)]$$

$$V_1 = L_1 I_c d(I_1/I_c)/dt + M I_c d(I_2/I_c)/dt, \quad [11(b)]$$

$$I_2 = I_c \sin \theta + V_2/R_2 + C_2 dV_2/dt, \quad [11(c)]$$

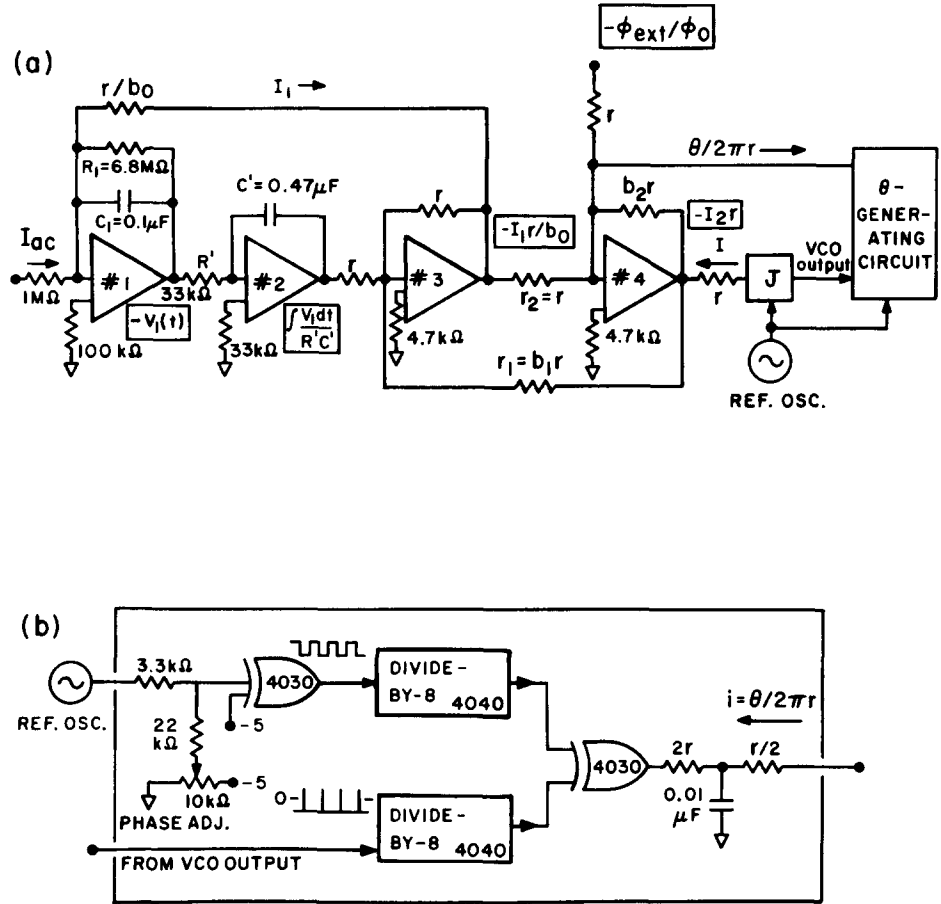
$$d\theta/dt = 2\pi V_2/\phi_0, \quad [11(d)]$$

and

$$\phi_{ext}/\phi_0 + (L_2 I_c/\phi_0) \times I_2/I_c + (M I_c/\phi_0) \times I_1/I_c + \theta/2\pi = 0. \quad [11(e)]$$

Here  $M$  is the mutual inductance between the tank cir-

FIG. 5. (a) Circuit analog of an rf SQUID. The tank circuit is modeled by op-amps 1, 2, and 3, the SQUID loop by a junction analog circuit ( $J$ ) as in Fig. 1(a), a circuit for generating a current proportional to  $\theta$ , and op-amp #4.  $r = 10 \text{ k}\Omega$ . Drive current  $I_{ac}$  is supplied by applying a sinusoidal voltage at the resonant frequency ( $\approx 10 \text{ Hz}$ ) to the left end of the  $1 \text{ M}\Omega$  resistor. The junction has its own  $\pm 5$  volt supply; all other integrated circuits are powered by a second  $\pm 5$  volt supply. Currents are denoted by arrows; voltage values are enclosed in boxes. For results shown later,  $r/b_0 = 100 \text{ k}\Omega$ . (b) Circuit for generating a current proportional to  $\theta$ , the phase difference between the VCO in the junction analog and the reference oscillator. As in the similar circuit of Fig. 3(b), the current is proportional to  $\theta$  only over the range  $-4\pi$  to  $+4\pi$ . The  $3.3 \text{ k}\Omega$  resistor helps isolate the reference oscillator from switching transients in the 4030. See Appendix A for component selection.



circuit coil and the SQUID loop. The first and third of these equations express Kirchhoff's current law in the tank circuit and in the RSJ model of the SQUID loop. The second equation gives the induced voltage drop across  $L_1$  due to  $I_1$  and  $I_2$ . The fourth is the Josephson voltage-phase relation and the fifth is the fluxoid quantization condition, analogous to Eq. [8(f)] for the double-junction SQUID.

The rf SQUID is modeled by the circuit of Fig. 5(a). This contains three op amps, #1, #2, #3, in a second-order loop which models the resonant tank circuit. With the component values shown in the figure and  $r/b_0 = 100 \text{ k}\Omega$ , the resonant frequency is about  $10 \text{ Hz}$  and the  $Q$  is about 30. The SQUID loop itself is modeled by the Josephson junction analog, Fig. 1(a), and a generator of a current proportional to  $\theta$  which is coupled back to the junction analog through op-amp #4. The magnetic coupling is modeled by the connections through resistors  $r_1$  and  $r_2$ .

The current proportional to  $\theta$  is obtained by a phase-sensitive detector [Fig. 5(b)] similar to the one used to produce  $\theta_2 - \theta_1$  in the double junction analog, except that the input to one of the counters is derived from the reference oscillator sine wave. This counter must be incremented at the precise instant the sine wave passes through zero with negative slope, which is accomplished by using one of the XOR gates in the CMOS 4030 as a sine wave to square wave converter with an adjustable phase difference. In operation, the phase is adjusted

(see Appendix A) to ensure that the average current supplied by the phase sensitive detector is zero when  $\sin \theta$  is zero.

Because a maximum voltage of 5 volts is produced when the VCO and the reference oscillator are  $4\pi$  radians out of phase, the average output current drawn by the XOR circuit from the inverting input of op-amp #4 through the resistor  $2r + r/2 = 2.5r$  is given by  $\theta/2\pi r$  over the range of proportionality. The reader may be curious as to why the current supplied by the phase sensitive detector is defined as positive when it flows away from the op amp in Fig. 5(a) but when it flows toward the op amp in Fig. 3(a). The answer is that in both circuits, under most circumstances, the phase difference between the square wave outputs of the divide-by-8 counters adjusts itself automatically, so that a slight deviation of  $\theta$  away from zero in either direction tends to be corrected back toward zero by current fed back from the phase sensitive detector. For further discussion of this point see Appendix A.

The equations governing the rf SQUID analog of Fig. 5a are as follows:

$$I_{ac} = I_1 + V_1/R_1 + C_1 dV_1/dt, \quad [12(a)]$$

$$\int V_1 dt / R'C' = I_1 r/b_0 + I_2 r/b_1,$$

or

$$V_1 = (R'C'r/b_0) dI_1/dt + (R'C'r/b_1) dI_2/dt, \quad [12(b)]$$

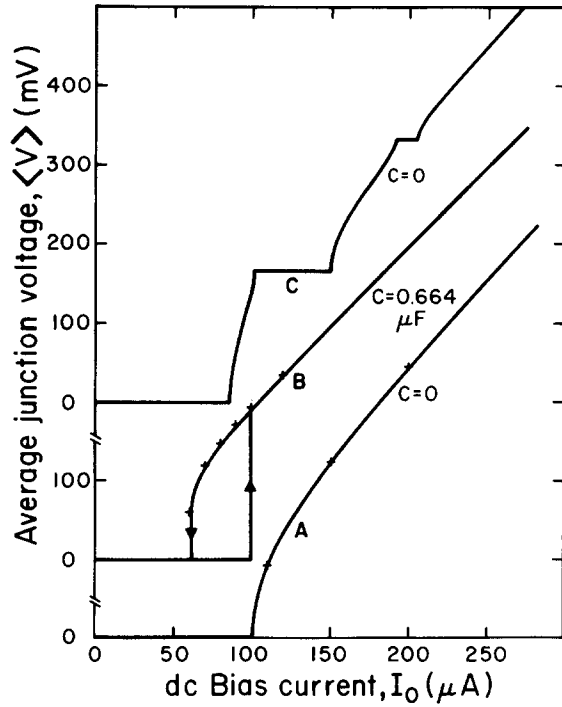


FIG. 6.  $I$ - $V$  characteristics for the analog of a single junction [Fig. 1(a)]. Curves B and C are offset vertically by 100 and 300 mV for clarity. The quasiparticle  $I$ - $V$  curve is a straight line through the origin with a  $45^\circ$  slope. Curve A: Junction capacitance  $C = 0$ . Crosses represent the values given by theory,  $\langle V \rangle = R(I_0^2 - I_c^2)^{1/2}$  for  $I_0 > I_c$ . Curve B: Junction capacitance  $C = 0.664 \mu\text{F}$ , for which  $\beta_c = 4.0$ . The crosses are taken from the computer-generated  $I$ - $V$  characteristics of McCumber, Ref. 3, Fig. 4, for  $\beta_c = 4.0$ . Curve C: Junction capacitance  $C = 0$ . In addition to the dc bias current, a 400-Hz sinusoidal current of amplitude (zero to peak)  $75 \mu\text{A}$  was applied to the inverting input of the op amp in Fig. 1(a) through an additional 10-k $\Omega$  resistor not shown in that figure.

$$I_2 = \sin \theta / r' + V_2 / R_2 + C_2 dV_2 / dt, \quad [12(c)]$$

$$d\theta / dt = 2\pi V_2 / \lambda, \quad [12(d)]$$

$$\phi_{\text{ext}} / \phi_0 + I_2 r / b_2 + I_1 r / b_0 + \theta / 2\pi = 0. \quad [12(e)]$$

Here  $r'$ ,  $R_2$ , and  $C_2$  are contained within the box labeled  $J$  in Fig. 5(a) [see Fig. 1(a)]. We emphasize that the  $R_2$  and  $C_2$  of the analog are *not* numerically equal to the  $R_2$  and  $C_2$  of the real rf SQUID. Also  $I_1$  and  $I_2$  in the analog may have values different from their counterparts in a real SQUID.

In order to make quantitative connections between constants and variables in the real SQUID and in the analog, we begin by comparing Eqs. [11(e)] and [12(e)] to make the following identifications:

$$I_2 / I_c \rightarrow I_2 r, \quad [13(a)]$$

$$L_2 I_c / \phi_0 \rightarrow 1 / b_2, \quad [13(b)]$$

where quantities for the analog are written on the right. Then from Eqs. [11(b)] and [12(b)] we must have

$$M I_c \rightarrow R' C' / b_1. \quad [13(c)]$$

Because we have previously made the identification  $\phi_0 \rightarrow \lambda$ , we can rewrite [13(c)] as

$$M I_c / \phi_0 \rightarrow R' C' / b_1 \lambda. \quad [13(c')]$$

If we now rewrite the third term in Eq. [12(e)] as  $(R' C' / b_1 \lambda) \times (b_1 \lambda r I_1 / R' C' b_0)$ , and compare it with the third term in Eq. [11(e)], namely  $(M I_c / \phi_0) \times I_1 / I_c$ , we can make the identification

$$I_1 / I_c \rightarrow (b_1 \lambda r I_1 / R' C' b_0). \quad [13(d)]$$

That is, the voltage  $b_1 \lambda r I_1 / R' C' b_0$ , which is proportional to the voltage at the output of op-amp #3 in Fig. 5(a), represents the normalized current  $I_1 / I_c$  in the tank circuit inductance of the real SQUID.

Finally, we compare the first term on the right of Eq. [12(b)], written in the form  $[(R' C')^2 / b_1 \lambda] \times d(b_1 \lambda r I_1 / R' C' b_0) / dt$  with the corresponding term in Eq. [11(b)],  $L_1 I_c d(I_1 / I_c) / dt$ , to obtain the further identification

$$L_1 I_c \rightarrow (R' C')^2 / b_1 \lambda, \quad [13(e)]$$

or

$$L_1 I_c / \phi_0 \rightarrow (R' C')^2 / b_1 \lambda^2. \quad [13(e')]$$

An important quantity in comparing our analog with a real rf SQUID is the dimensionless ratio  $k^2 = M^2 / L_1 L_2$ . This ratio must be less than 1. For our analog  $k^2$  can be obtained by combining [13(b)], [13(c')], and [13(e')], to obtain

$$k^2 = b_2 / b_1. \quad (14)$$

### III. RESULTS

#### A. Current-biased single junction

In Fig. 6 we show curves of average junction voltage  $\langle V \rangle$  as a function of dc bias current  $I_0$ , taken with the single junction analog of Fig. 1 with  $R = 2.00 \text{ k}\Omega$ , and  $r' = 10.0 \text{ k}\Omega$ , so that the critical current for the junction analog is  $100 \mu\text{A}$ . The crosses on curve A (junction capacitance  $C = 0$ ) are points calculated from the analytically-derived equation (see, for example, Stewart and McCumber, Ref. 3).

$$\langle V \rangle = R(I_0^2 - I_c^2)^{1/2}. \quad (15)$$

When the junction capacitance is different from zero the amount of hysteresis is determined by the dimensionless quantity  $\beta_c \equiv 2\pi I_c R^2 C / \phi_0 \rightarrow 2\pi R^2 C / r' \lambda$ . For curve B the junction capacitance was  $0.664 \mu\text{F}$ ; with  $R = 2.00 \text{ k}\Omega$ ,  $r' = 10.0 \text{ k}\Omega$ , and  $\lambda = 4.125 \times 10^{-4} \text{ V s}$ ,  $\beta_c = 4.0$ . Since an analytical computation of the  $I - \langle V \rangle$  curves for a junction with hysteresis has not been accomplished, the crosses are taken from the corresponding computer-generated curve of McCumber's Fig. 4 (Ref. 3) for  $\beta_c = 4.0$ . This fit is in fact much better than that achieved with a  $\sin \theta$  circuit consisting of a mixer and a low pass filter.<sup>13</sup> (In the analog of Ref. 13 an experimental value of  $\beta_c = 5$  produced the best fit to McCumber's curve for  $\beta_c = 4.0$ .) The improvement of our sampling circuit in modeling the dynamic behavior of a junction is a significant advantage of the sampling circuit, and is of particular importance when more complex SQUID circuits are considered.

For curve C we added, through an additional input resistor to the negative input of the op amp, a sinusoidal bias current of zero-to-peak amplitude  $75 \mu\text{A}$  and fre-

quency 400 Hz. We thus obtain the familiar Shapiro steps.<sup>9</sup> For this curve the junction capacitance is zero. Curve C is useful because the voltage interval between steps is  $hf/2e$  in a real junction and  $\lambda f$  in the analog; thus we find  $\lambda = 0.165 \text{ V}/400 \text{ Hz} = 4.125 \times 10^{-4} \text{ V s}$ .

Table I lists certain parameters of importance in describing real junctions and gives the corresponding quantity in the analog along with its numerical value.

## B. Double-junction SQUID

For the double-junction SQUID two types of characteristics are of interest, static and dynamic. The limits of static behavior, in which there may be supercurrent but the junction voltages are zero, are defined by curves of critical current of the SQUID as a function of the external magnetic flux through the SQUID loop. Critical current curves, taken with the analog circuit of Fig. 3, are shown in Fig. 7 for two sets of values of  $L_1 I_c / \phi_0$  and  $L_2 I_c / \phi_0$ . In the curve of Fig. 7(a) the "SQUID" is symmetric with  $L_1 I_c / \phi_0 = L_2 I_c / \phi_0 = 0.50$ , while in Fig. 7(b) the "SQUID" is asymmetric, with  $L_1 I_c / \phi_0 = 0.10$ , and  $L_2 I_c / \phi_0 = 0.50$ . Similar computer-generated curves have been obtained by Tesche and Clarke.<sup>14</sup>

These critical current curves are most easily plotted by setting the dc bias current to a particular value and then varying the external flux. Two different behaviors are observed. In Fig. 7(a) for a bias current such as  $170 \mu\text{A}$  the junctions either have voltage across them (above the solid curve) or they do not (below the solid curve). However, for a bias current such as  $100 \mu\text{A}$  the junction voltages are zero for all values of external flux; the cross-

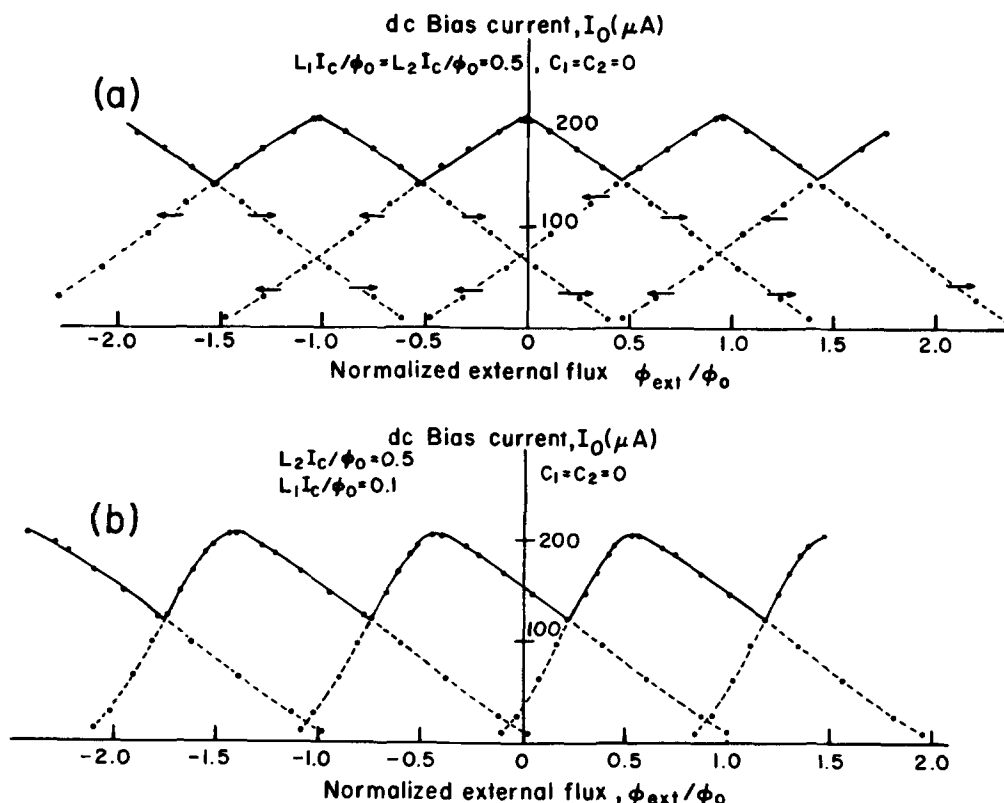
TABLE I. Values of circuit parameters for junction analog.

Real junction	Analog	Value
$I_c$	$1.00\text{V} \times (1/r')$	$100 \mu\text{A}$
$R$	$R$	$2.00 \text{ k}\Omega$
$\phi_0$	$\lambda$	$4.125 \times 10^{-4} \text{ V s}$
$I_c R$	$1.00\text{V} \times (R/r')$	$200 \text{ mV}$
$I_c R / \phi_0$	$1.00\text{V} \times (R/r'\lambda)$	$485 \text{ Hz}$
	frequency of Ref. osc.	$110 \text{ kHz}$
	amplitude of Ref. osc.	$1.00 \text{ V zero to peak}$

ing of one of the dotted curves, marking the lobe boundaries, in the direction shown by arrows, is signaled by abrupt changes in  $\theta_2 - \theta_1$ ,  $\sin \theta_1$ , and  $\sin \theta_2$ , and by brief voltage pulses across the junctions themselves. These abrupt changes result from a flux quantum suddenly entering or leaving the SQUID loop.

To examine the dynamic behavior of the double-junction SQUID we can display the time-dependent junction voltages  $V_1$  and  $V_2$  and supercurrents  $\sin \theta_1 / r'$  and  $\sin \theta_2 / r'$ , and can plot curves of the time-average voltage  $\langle V \rangle$  across the SQUID as a function of the bias current  $I_0$ . The time-dependent waveforms cannot be observed in a real SQUID because they vary at microwave frequencies. In the analog there is no point in the circuit that provides the sum of the voltage across a junction plus the voltage across the corresponding inductance. However, we are interested in the time-average voltage across the loop, and this is equal to the time-average voltage across either junction. This equivalence is due to the fact that the voltage across a self-inductance or mutual

FIG. 7. Critical current vs external flux  $\phi_{\text{ext}}/\phi_0$  for double-junction SQUID analog. Each curve was generated by fixing the dc bias current  $I_0$  [actually the voltage  $rI_0$  in Fig. 3(a)] and varying  $\phi_{\text{ext}}/\phi_0$  to determine the boundaries either between the zero voltage state of the junctions and the nonzero voltage state (solid curves) or between zero voltage states with different numbers of flux quanta trapped in the SQUID loop (dashed curves). The arrows on the dashed curves show the direction in which the flux was changed to observe the transition between trapped flux states. (a) Nominally equal inductances  $L_1 I_c / \phi_0 = L_2 I_c / \phi_0 = 0.5$ ;  $C_1 = C_2 = 0$ . (b) Unequal inductances  $L_1 I_c / \phi_0 = 0.1$ ;  $L_2 I_c / \phi_0 = 0.5$ ;  $C_1 = C_2 = 0$ .





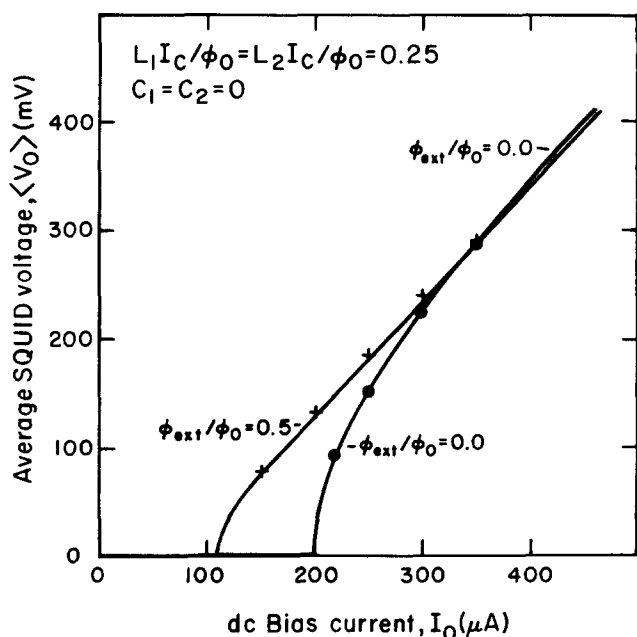


FIG. 8. Average voltage  $\langle V_0 \rangle$  of double-junction SQUID vs total bias current  $I_0$  with  $C_1 = C_2 = 0$ , for two different values of externally applied flux,  $\phi_{\text{ext}}$ . The actual plotted voltage is  $\langle V_2 \rangle$ , which is equal to  $\langle V_0 \rangle$ . The crosses and circles are taken from the computer-generated curves of Tesche and Clarke, Ref. 14, Fig. 6(a). The values  $L_1 I_c / \phi_0 = L_2 I_c / \phi_0 = 0.25$  correspond to  $\beta = 1$  of Ref. 14. The crossing of the two curves at  $\langle V_0 \rangle \approx 300$  mV is not seen in the digital simulations of Ref. 14. This crossing apparently results from time delays in the analog circuit, Fig. 3; see text.

inductance is proportional to the rate of change of the current, and the average rate of change of a periodic quantity such as  $I_1$  or  $I_2$  over any number of periods is zero.

Figure 8 shows  $I$ - $V$  curves for a symmetric double-junction SQUID with  $L_1 I_c / \phi_0 = L_2 I_c / \phi_0 = 0.25$  and  $C = 0$ . The crosses are taken directly from the computer-generated characteristics in Fig. 6(a) of Tesche and Clarke.<sup>14</sup> Except for the crossing of our SQUID analog curves for  $\phi_{\text{ext}}/\phi_0 = 0$  and  $\phi_{\text{ext}}/\phi_0 = 0.5$ , which does not occur in Tesche and Clarke's curves, the agreement is quite good. We believe that the crossing is an artifact caused by time lag in the phase detector due to the  $0.01 \mu\text{F}$  smoothing capacitor and to the inherent delay in dividing the VCO frequencies by 8. Each effect contributes a time lag of  $\sim 40 \mu\text{s}$ . This delay is unavoidable because the times at which the XOR inputs switch their logic states depend on  $d\theta_1/dt$  and  $d\theta_2/dt$  and hence the junction voltages over the previous four periods of the VCOs. The fact that the crossing occurs at a lower value of  $I_0$  when the phase detector capacitor is increased to  $0.1 \mu\text{F}$  supports this interpretation, as does the fact that the crossing nearly disappears if divide-by-4 counters replace the divide-by-8 counters. (This change in counter ratio requires that the  $2.5 r$  resistance in the phase detector be increased to  $5 r$  in order that the average current remain equal to  $(\theta_2 - \theta_1)/2\pi r$ .) The value of the smoothing capacitor used in the phase detector circuit, Fig. 3(b),  $0.01 \mu\text{F}$ , cannot be reduced very much because otherwise the ac signal will not be adequately filtered and the output of op-amp #1 will saturate.

The  $I$ - $V$  curves in Fig. 9 show the interesting behavior that can occur for finite capacitance. In this case  $C = 0.664 \mu\text{F}$  for each junction, which corresponds to  $\beta_c = 4.0$ . The curve for  $\phi_{\text{ext}}/\phi_0 = 0$  has two branches. The upper branch is identical to the single junction curve (Fig. 6, curve B), except that the total current is twice the individual junction current. For the upper branch, corresponding currents and voltages in the two junctions are in phase and the total flux in the loop is zero at all times. The lower branch is reached by momentarily applying a nonzero external flux while the bias current is fixed at some value between about 130 and 180  $\mu\text{A}$ . In this lower branch the corresponding currents and voltages in the two junctions are out of phase. There is a nonzero circulating current in the SQUID loop in this case, and flux quanta alternately enter and leave the loop. Waveforms of  $\sin \theta_1(t)$  and  $\sin \theta_2(t)$  are shown in Fig. 10 for a total bias current  $I_0 = 180 \mu\text{A}$ . The upper two curves in Fig. 10 are for the upper branch of the  $\phi_{\text{ext}} = 0$  characteristic. The bottom two curves show the out-of-phase behavior for the lower branch. It is not clear whether this out-of-phase behavior is a stable solution for exactly matched junctions with  $\phi_{\text{ext}}$  exactly zero. The stability and accessibility of this so-called beating solution is currently under theoretical investigation.<sup>15</sup>

For the upper curve in Fig. 9 the external flux was half a flux quantum,  $\phi_{\text{ext}}/\phi_0 = 0.5$ . The  $I$ - $\langle V \rangle$  characteristic is distinguished by two distinct ranges of bias current for which hysteresis occurs.

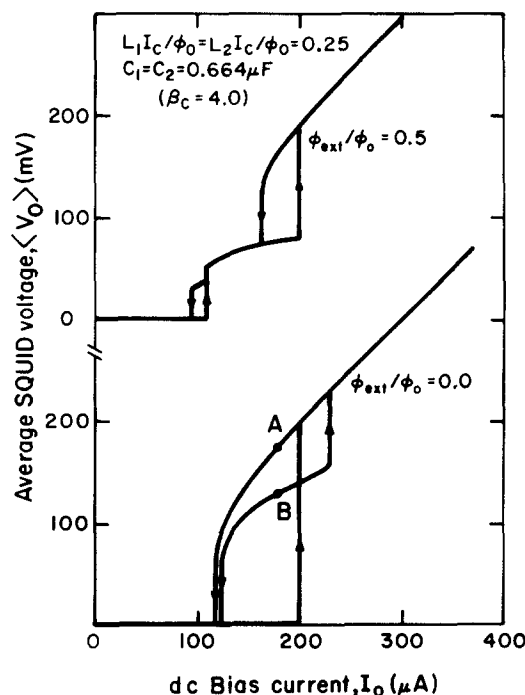


FIG. 9. Average SQUID voltage  $\langle V_0 \rangle$  as a function of bias current  $I_0$  with junction capacitances of  $0.664 \mu\text{F}$ , which correspond to  $\beta_c = 4.0$ . The curve for  $\phi_{\text{ext}} = 0$  has two branches, the lower of which is accessed by momentarily applying a nonzero value of  $\phi_{\text{ext}}$  (see text). The curve for  $\phi_{\text{ext}} = 0.5 \phi_0$  has two regions of bias current in which hysteresis occurs. Arrows indicate regions where the SQUID voltage jumps from one value to another.

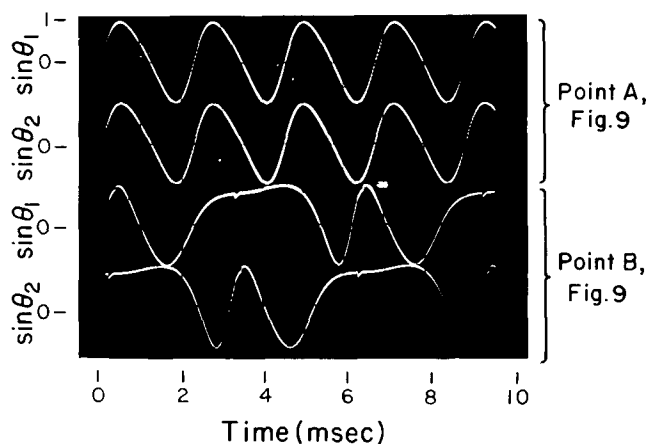


FIG. 10. Graphs of supercurrent vs time for the double-junction SQUID analog. Conditions are as in Fig. 9, with  $\phi_{\text{ext}}/\phi_0 = 0.0$  and the dc bias current  $I_0 = 180 \mu\text{A}$ . Top two curves:  $\sin \theta_1$  and  $\sin \theta_2$  for the upper branch, point A in Fig. 9. Bottom two curves:  $\sin \theta_1$  and  $\sin \theta_2$  for the lower branch, point B in Fig. 9.

### C. Radio-frequency SQUID

In Figs. 11 and 12 we present results for the rf SQUID analog (Fig. 5) for the two standard ways of illustrating the behavior of an rf SQUID. We set  $C_2 = 0$ ,  $L_2 I_c / \phi_0 = 0.5$ , and  $k^2 = b_2/b_1 \approx 0.029$ .

In Fig. 11 we plot the rms voltage  $V_1$  across the tank circuit as a function of the applied external flux  $\phi_{\text{ext}}$  with the rms value of the rf drive current  $I_{\text{ac}}$  held constant. The curve is extended to the largest values of  $\phi_{\text{ext}}$  permitted by the circuit model. Use of larger values of external flux causes the angle  $\theta$  to deviate from zero by more than  $4\pi$ , as in Fig. 3(c), at least at some point in the cycle, so that the current output of the  $\theta$ -generating circuit is no longer proportional to  $\theta$ . In the actual operation of a real rf SQUID the SQUID loop is biased with external flux to give an extremum of tank circuit voltage. In addition, the flux is modulated at a low frequency  $f_1$  causing the tank circuit voltage to vary at a fundamental frequency of  $2f_1$ . An additional small unknown dc flux causes the detected tank circuit voltage to acquire a component at frequency  $f_1$ , whose amplitude, usually measured with a lock-in amplifier, is proportional to this unknown flux.

FIG. 11. Time-average rms tank circuit voltage,  $V_1$ , as a function of the external flux  $\phi_{\text{ext}}/\phi_0$  in the rf SQUID analog of Fig. 5. The drive current frequency is 10.6 Hz and its amplitude is  $0.18 \mu\text{A}$  (zero to peak).  $V_1$  is measured with a digital ac voltmeter.

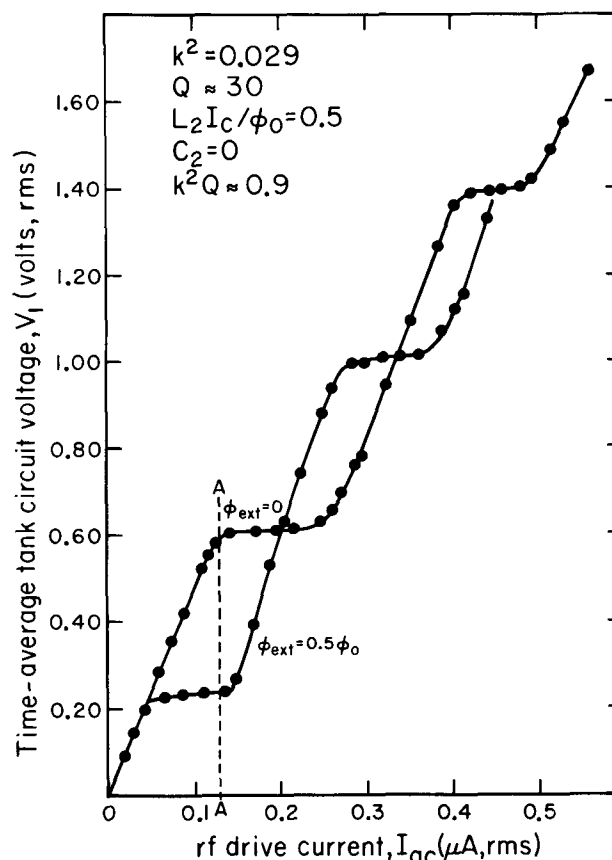
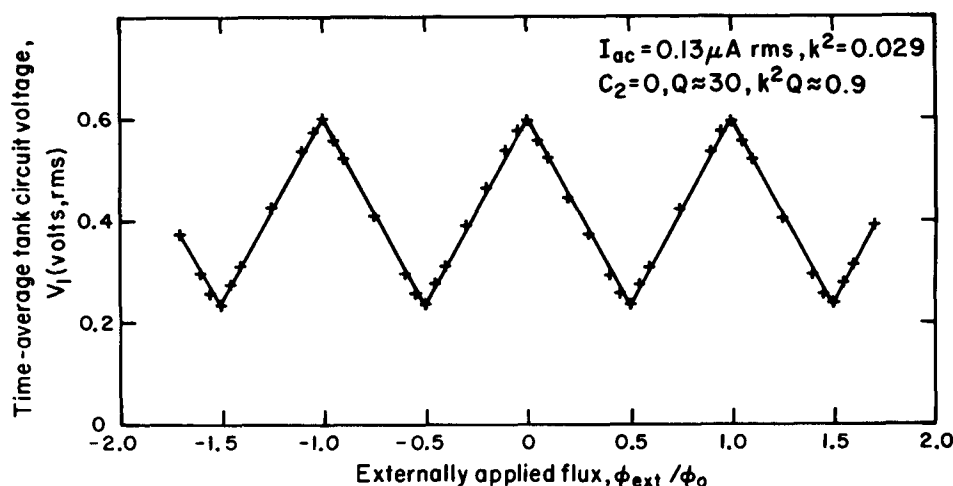


FIG. 12. Time-average rms tank circuit voltage  $V_1$  as a function of drive current  $I_{\text{ac}}$  for two different values of external flux. A marks the drive current used in obtaining Fig. 11.  $V_1$  and  $I_{\text{ac}}$  are measured with digital ac voltmeters.

Figure 12 shows curves of tank voltage vs drive current  $I_{\text{ac}}$  taken with the analog for two values of external flux,  $\phi_{\text{ext}} = 0$  and  $\phi_{\text{ext}} = 0.5 \phi_0$ . The rms values of  $I_{\text{ac}}$  and  $V_1$  were measured with digital ac voltmeters. Clearly evident are an interleaved sequence of "steps and risers" caused by the energy dissipation mechanism discussed in Sec. II(c). The curves of Figs. 11 and 12 compare favorably with results for real SQUID devices.<sup>16</sup>

### IV. DISCUSSION

In summary, we have shown how to construct electronic analogs of double- and single-junction SQUIDs

based on an analog of a resistively shunted Josephson junction. Several of the novel features of our single junction and SQUID analogs represent significant improvements over previous work and should be applicable in a wider variety of situations than described in the present article. The method of summing the supercurrent, quasiparticle current, and displacement current in a single op amp is a major simplification over analogs [for example, Bak and Pederson (Ref. 5)] in which the  $\sin \theta$  current is produced by a voltage-to-current converter. The low cost of the circuit components and the simplicity of the single-junction analog should encourage the modeling of arrays of junctions. It seems likely that only one reference oscillator would be required in such multiple-junction circuits. A further advantage of the sampling-type analog we have described is its superior dynamic performance, as compared with the mixer-low pass filter type used by Bak and Pederson.<sup>5</sup> The sampling method also allows one to model a nonsinusoidal current-phase relation [replacing Eq. (1)] by using a waveform from a function generator whose voltage-time relation is the desired  $I(\theta)$  relation. Indeed, any periodic waveform that can be obtained with a function generator or synthesizer (for example, a sawtooth wave) could replace the sinusoidal reference wave.

A useful and general technique demonstrated in these analogs is the modeling of inductance by using op amps to enforce the fluxoid quantization condition. Circuits which simulate the behavior of ideal inductors, with zero resistance (see Ref. 7), are therefore not required. Our method requires a current proportional to a phase difference. The divide-by-8 counters which enable us to generate this current could in principle be divide-by-16, 32, or more. However, the increased time delay, or lag, involved in this method of measuring phase differences limits its use to situations in which changes in phase occur slowly compared with the period of the counter outputs. While this problem might be circumvented by running the reference oscillator and VCO at higher frequencies, the absolute frequency stability of the oscillators must not degrade if the characteristic junction frequency ( $\sim R/r'\lambda$ ) is left unchanged. That is, a 1-MHz oscillator rate would permit the phase information to be updated ten times as often as a 100-kHz rate. However, the fractional long term drift and short term jitter, about 1 or 2 parts in  $10^5$  with the circuit components we used, would have to be improved to 1 or 2 parts in  $10^6$  if the faster oscillator were used in order to maintain accurate sampling of  $\sin \theta$ . If it is possible to obtain higher frequency VCO's with satisfactory frequency stability, there should be no problem in generating a sinusoidal reference wave of the required stability from a crystal oscillator. While the sample-hold circuit employed here might prove inadequate at higher frequencies, sample-hold modules with much faster acquisition times are readily available from several manufacturers.<sup>17</sup>

An area of considerable scientific and technical interest which we have not explored in this paper is the

effect of noise on the SQUID characteristics. Extensive and careful digital calculations of noise effects in both the double-junction<sup>14</sup> and single-junction<sup>16</sup> SQUID have been presented. It appears that Johnson noise in the junction resistances  $R$  could be simulated with random noise generators. It is not clear, however, how to introduce noise corresponding to quantum fluctuations.<sup>14</sup> The electronic analog does contain noise of its own due to noise in the op amps, frequency-, and amplitude jitter of the reference oscillator and frequency jitter of the VCOs, etc. However, the experimental  $I$ - $V$  curves of Figs. 6 and 8 show little or no evidence of noise rounding and the results presented appear to correspond closely to those of the noise-free calculations.

One of the most useful features of the SQUID analogs described here is their ability to display time-varying waveforms which in the real SQUID vary too rapidly for present-day instruments, such as fast sampling oscilloscopes, to display. For example, there appears to be a great deal of interesting behavior involving self-resonances and mixing of harmonics of the Josephson frequencies in multiple-junction interferometer circuits.<sup>18</sup> Analog circuits based on the techniques we have described should permit these circuit properties to be investigated over a wide range of circuit parameters in a fraction of the time required for digital computations.

## ACKNOWLEDGMENTS

We wish to thank S. Grodzinsky, A. Davidson, and S. M. Faris for useful discussion on various aspects of this work, and Y. Imry for communicating results prior to publication. This research was supported in part by NSF Grants ENG 77-10164 and ECS 79-27165. The provision of a sabbatical leave by Bucknell University and the hospitality of the Department of Engineering and Applied Science at Yale University is gratefully acknowledged by one of us (R.W.H.).

## APPENDIX A: CONSTRUCTION AND ADJUSTMENT PROCEDURES

In this Appendix we point out several items relating to construction and adjustment of the various analog circuits.

### A. Adjustment of the VCOs

The VCO circuits, made from 555 timers [Fig. 1(d)], must include 10- or 20-turn trimpots for adjusting their center frequencies. Alternatively, if the reference oscillator is adjustable, only one of the VCO frequencies needs to be adjustable. In operation, after allowing a few minutes for warmup, one adjusts the frequency of each VCO individually to equal that of the reference oscillator. This is done by placing switches  $S_1$  [Fig. 1(a)],  $S_2$ , and  $S_3$  [Fig. 3(a)] in their grounded positions to break all feedback connections. Then the VCO center frequency is adjusted, while observing the beats of the  $\sin \theta$  waveform, until the beat frequency is as close to zero as possible.

During construction, the slopes of the frequency-voltage characteristics of the two VCOs must also be carefully matched so that  $\lambda$ , the analog of the flux quantum  $\phi_0$ , is the same in the two junction analogs. To do this, begin with a somewhat larger resistor, e.g., 100 k $\Omega$ , in place of the 82.5 k $\Omega$  resistor in Fig. 1(d) for one of the junction analogs and then add an appropriate resistance in parallel that gives Shapiro steps (Fig. 6, curve C) with the same step separation as in the other junction analog.

## B. Power supply filtering and shielding

The main impediments to high quality performance of the analog circuits are unwanted interactions among the two or three oscillators. For this reason each junction analog (Fig. 1) has its own pair of  $\pm 5$  volt regulators, as shown in Fig. 13. These are separate from the  $\pm 5$  volt regulators that power the remaining circuitry. Also, within each junction analog circuit it is helpful to use RC decoupling filters in the power supply leads to the various integrated circuits. (For example,  $R = 27 \Omega$ ,  $C = 6.8 \mu\text{F}$ .) To prevent capacitive interactions the leads to and from the VCOs and from the reference oscillator are kept short, and where that is not possible, shielded cable is used. In our work, each junction analog was mounted within its own shielded aluminum box, and BNC connectors and cables were used for interconnections.

Unwanted interactions within each junction analog can be diagnosed by the beats of  $\sin \theta$ , observed during the frequency-adjustment process, being sawtooth rather than sinusoidal functions of time. Interactions between the VCOs of the two analogs can be seen as a tendency of one VCO to lock to the other when neither is locked to the reference oscillator. If a common  $\pm 15$  volt supply is used to power all  $\pm 5$  volt regulator circuits, it helps to put a small resistance, e.g., 47  $\Omega$ , in series with the input of each regulator (see Fig. 13).

## C. Trimming the $\theta_2 - \theta_1$ circuit

For greatest accuracy in satisfying Eqs. [9(e)] and [9(f)] the outputs of op-amps #1, #2, and #3 in the double-junction SQUID analog should be trimmed to give zero when  $\theta_1 = \theta_2 = 0$  and when all other inputs to these op amps are zero. To make this adjustment the voltage  $\phi_{\text{ext}}/\phi_0$  is set to zero and switch  $S_2$  is placed in the grounded position. Also, either one (but not both) of the inputs to the XOR circuit from the divide-by-8 counters is disconnected and reconnected to either supply voltage, so that the output of the XOR is a square wave of precisely 50% duty cycle. Finally the offset null pots for op-amps #1, #2, and #3 are adjusted, in that order, to give zero output from each op amp.

## D. Adjusting the phase in the $\theta$ circuit of the rf SQUID analog

The phase of the square wave derived from the reference oscillator sine wave must be adjusted, so that the

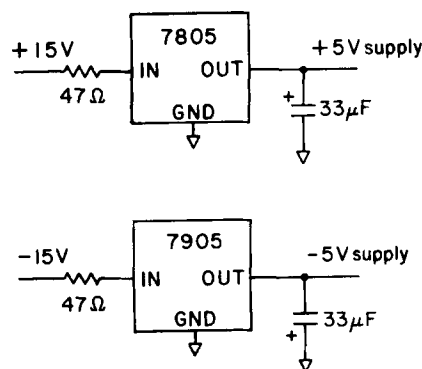


FIG. 13. Power supply circuits for the electronic analogs. Each junction analog employs a separate pair of 7805 and 7905 regulators. Other integrated circuits are powered by an additional  $\pm 5$  volt supply. Additional RC decoupling filters ( $R = 27 \Omega$ ,  $C = 6.8 \mu\text{F}$ ) are included, as needed, in the connections to individual integrated circuits.

current fed back to op-amp #4 is zero when the phase difference  $\theta$  between the reference oscillator and the VCO is zero. The easiest way to do this is to set  $\phi_{\text{ext}}/\phi_0$  to zero and to disconnect the coupling resistor  $r_2$  in Fig. 5(a). Next the switch  $S_1$  in the junction analog is put in its grounded position to remove the  $\sin \theta$  feedback. Now the junction analog, the  $\theta$  circuit, and op-amp #4 are in a phase-locked-loop configuration and, provided the VCO and reference oscillator frequencies are matched, the output of op-amp #4 will automatically adjust to zero. However, the  $\sin \theta$  voltage may not be zero; it is adjusted to zero by trimming the phase adjustment pot, Fig. 5(b), until the  $\sin \theta$  voltage in the junction analog, Fig. 1(a), is zero.

## E. Filtering the junction voltages

The time-average junction voltage is required for some of the characteristic curves. To obtain this average we use simple RC low pass filters with  $R = 1 \text{ k}\Omega$  and  $C = 10 \mu\text{F}$  to give a smoothing time constant of  $10^{-2}$  s. Any remaining ripple is ignored by our  $x$ - $y$  recorder.

## F. Component selection

Metal film resistors were used for all critical resistances, or where matched values of 10 k $\Omega$  were required. Corning type RN60D metal film resistors, with  $<100$  ppm/ $^{\circ}\text{C}$  temperature variation, were used. Silver mica capacitors were used in the  $\sin \theta$  circuit [Fig. 1(b) and (d)]. Operational amplifiers were standard type 741 op amps. Because of the significant offset currents of these op amps, compensating resistors were used between the positive terminal and ground in each inverter circuit. To reduce further both drifts and temperature dependent offsets, it would be of advantage to use one of the improved versions of the type 741 amplifier, available for example, from Analog Devices,<sup>17</sup> or a low-drift operational amplifier.

We have found that some CMOS 4066 switches in the  $\sin \theta$  circuit of Fig. 1(b) have output offset voltages of order 10 mV during their off cycle. This can lead to an offset of some mV in the voltage stored on the capacitor

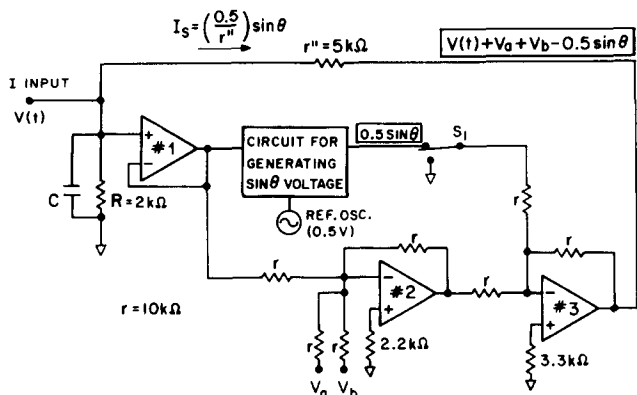


FIG. 14. Single-junction analog in which the junction current  $I$  is applied at the same point as that at which the junction voltage is measured. Op amps are type 741. Junction resistance  $R = 2 \text{ k}\Omega$  and junction capacitance  $C$  are shown. The voltage-to-current converter, to draw a  $\sin \theta$  "supercurrent" from the junction terminal, consists of op-amps #2 and #3. (The critical current,  $I_c$ , is  $100 \mu\text{A}$ , as in the junction analog of Fig. 1.) In addition, the junction may be current biased by applying voltages to inputs  $V_a$  or  $V_b$ .

$C_0$ , thereby producing apparent bias current offsets of  $\approx 1 \mu\text{A}$ . If this offset is of concern, it may be nulled by injecting a compensating current into the negative terminal of the op amp, Fig. 1(a), through a  $1\text{-M}\Omega$  resistor.

## APPENDIX B: "TWO-TERMINAL" JUNCTION ANALOG

In the single-junction analog of Fig. 1 used throughout this paper, the junction current is applied at a different terminal than the point where the junction voltage is developed. In certain applications one may require a single-junction analog in which the junction current is injected at the same point as that where the junction voltage is measured. An example is the study of interactions with a resonant circuit in series with the junction. We therefore present in this Appendix a configuration in which the voltage and current are measured at the same terminal.

A schematic diagram of the circuit is given in Fig. 14. This circuit uses the same method for generating the  $\sin \theta$  voltage as Fig. 1(b). However, as in Bak and Pederson,<sup>5</sup> the  $\sin \theta$  circuit is followed by a voltage-to-current converter, made up of op-amps #2 and #3. If  $V_a = V_b = 0$ , the output voltage of op-amp #3 is equal to  $V - 0.5 \sin \theta$ , with  $V$  the junction voltage. The amplitude of the reference oscillator is here adjusted to be 0.5 volts zero to peak. The current  $I_s$  drawn from the junction terminal is therefore equal to  $(0.5/r'') \sin \theta$  (again for  $V_a = V_b = 0$ ). As a result, the circuit of Fig. 14 satisfies Eq. (3) for the total junction current, with  $I_c = 100 \mu\text{A}$ .

The other inputs to the voltage-to-current converter,  $V_a$  and  $V_b$ , may be used to current bias the junction with

dc and/or ac currents equal to  $(V_a + V_b)/r''$ . Since the VCO circuit, Fig. 1(d), has an input resistance of  $82.5 \text{ k}\Omega$ , a unity-gain buffer, op-amp #1, is used to prevent loading of the junction. The full circuit in Fig. 14 is seen to be more complicated than that in Fig. 1, due to the more complex current summation method used. However, it still represents an improvement over the original Bak and Pederson circuit,<sup>5</sup> because of the improved method used for generating the  $\sin \theta$  voltage.

<sup>a1</sup> Permanent address.

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